64000

HP64000 Logic Development System

Model 64192A 6805 R/U Emulator Pod

HEWLETT PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard system product is warranted against defects in materials and workmanship for a period of 90 days from date of installation. During the warranty period, HP will, at its options, either repair or replace products which prove to be defective.

Warranty service of this product will be performed at Buyer's facility at no charge within HP service travel areas. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses. In all other cases, products must be returned to a service facility designated by HP.

For products returned to HP for warranty service. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

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THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

CW&A 2/81

HEWLETT-PACKARD

SERVICE MANUAL

MODEL 64192A

6805 R/U EMULATOR POD

REPAIR NUMBERS

This manual applies directly to models
with repair numbers prefixed 2301A.

Manual Part Number: 64192-90901
Microfiche Part Number: 64192-90801

Printed: January 1983

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

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SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual supports board level servicing of the Hewlett-Packard Model 64192A 6805 R/U Emulator Pod. Detailed operating instructions are provided in a separate operating manual supplied with the instrument. Because the emulator pod cannot run without a control board, this manual also includes installation and testing procedures for the Hewlett-Packard Model 64191A 6805 Emulator Controller.

1-3. Described in this section are instruments covered, the general features of the emulator pod, power supply loads, and its use with the Hewlett-Packard Model 64191A 6805 Emulator Controller. Also included are conventions used in the manual.

1-4. Shown on the title page is a microfiche part number. This number can be used to order 4 x 6 inch microfilm transparencies of the manual. Each microfiche contains up to 96 photoduplicates of the manual pages.

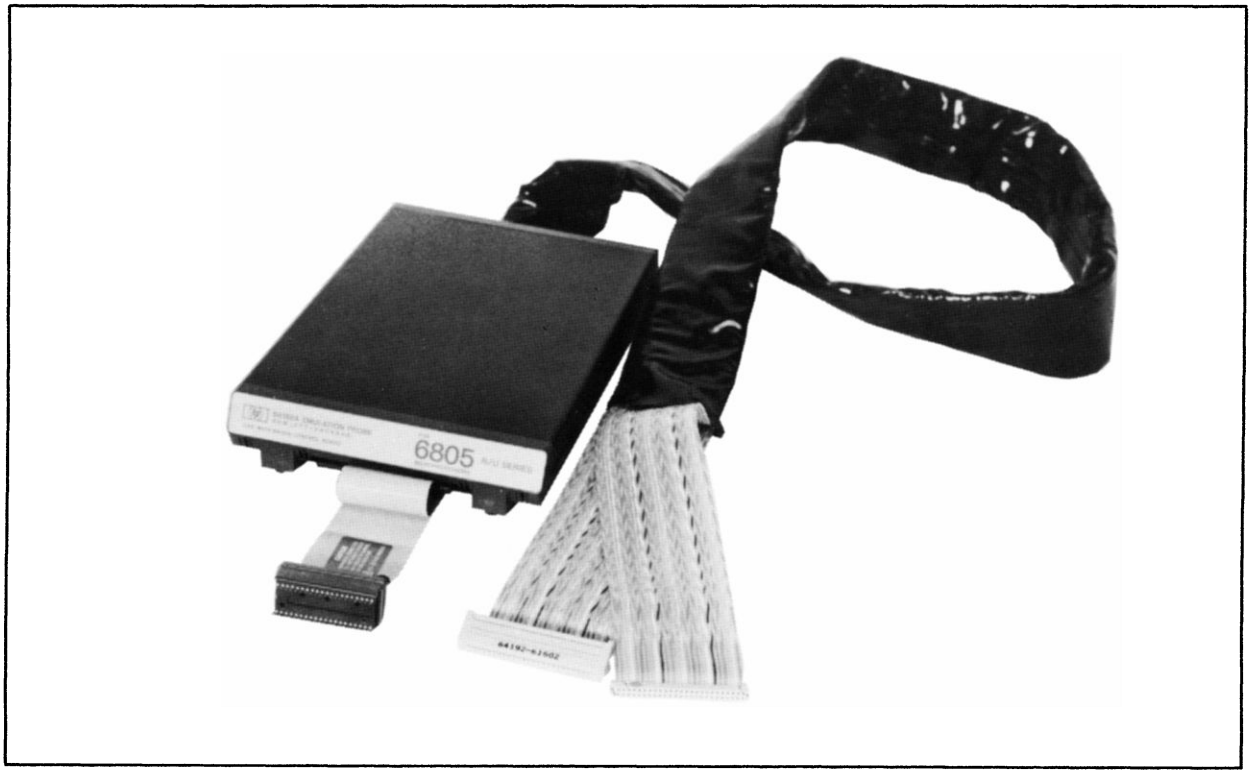


Figure 1-1. 6805 R/U Emulator Pod (Probe)

1-5. RELATED SERVICE MANUALS.

1-6. Table 1-1 shows the topics covered in the emulator pod and emulator controller service manuals. Service manuals for the models listed below provide additional information.

a. Development station models 64100A and 64110A.

b. Internal analyzer models 64300A and 64302A.

Table 1-1. 6805 R/U Emulator Subsystem Service Manuals

Subject	Model 64191A Emulator Controller Service Manual	Model 64192A Emulator Pod Service Manual
General information	yes	yes
Installation	yes	yes
Operation	no, see op manual	no, see op manual
Testing	no, see pod	yes, control & pod
Adjustments	no, none required	no, none required
Parts list	yes, control only	yes, pod only
Service schematics and theory	yes, control only	yes, pod only

1-7. INSTRUMENTS COVERED BY THIS MANUAL.

1-8. Attached to the Model 64192A 6805 R/U Emulator Pod is a repair number tag. The repair number is in the form 0000A 00000. It is in two parts; the first four digits and the letter are the prefix and the last five are the suffix. The prefix is the same for each identical 64192A 6805 R/U Emulator Pod; it only changes when a change is made to the pod. The suffix is assigned sequentially and is different for each model 64192A manufactured. This manual applies to each model 64192A with a repair prefix that is listed on the title page.

1-9. A model 64192A manufactured after the printing of this manual may have a repair number not listed on the title page. The manual for the newer emulator pod is accompanied by a yellow manual change supplement. The supplement explains how to adapt the manual to the newer emulator pod.

1-10. In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest manual changes supplement. The supplement is identified by the manual print date and part number, both of which appear on the manual title page. Copies are available at the Hewlett-Packard sales/service offices listed in the back of this manual.

1-11. DESCRIPTION.

1-12. Emulation of 6805 R/U microcomputers is provided by an emulation subsystem consisting of a Model 64191A 6805 Emulator Controller, a Model 64192A 6805 R/U Emulator Pod, and emulator software. See figure 1-1. The emulator controller is installed in a Hewlett-Packard 64000 series development station and connected to the emulator pod. The probe at one end of the emulator pod can be connected to the user's target system hardware.

1-13. The products in the MC6805 R/U family are single-chip microcomputers with their architecture optimized for controller applications. They have the basic MC6800-type microprocessor unit, clock oscillator, timer, ROM, RAM, or EPROM, and I/O control, all located on the 40 pin microcomputer package. The microcomputers communicate with the outside world through eight bit ports and have various user-specified options that can be hardware masked during manufacture. See table 1-2.

1-14. EMULATION FEATURES.

1-15. Prior to running user programs, the emulator software prompts the user to select certain microcomputer characteristics. These characteristics include choices that relate to target system hardware design and the 6805 microcomputer to be emulated. For example, the user can choose emulation of the following 6805 microcomputers:

MC6805R2 MC68705R3 MC6805U2 MC68705U3

1-16. The 6805 microcomputer clock source can be either an internal 4 MHz crystal located on the pod, or target system clock hardware.

1-17. Depending on the microcomputer, the timer clock can be on, off, external, or internal_gated. In addition, the timer prescaler has 8 user selectable values.

Table 1-2. MC6805 R/U Feature Summary

	6805R2	68705R3	6805U2	68705U3
On-chip EPROM	no	3.8K	no	3.8K
On-chip RAM	64	112	64	112
On-chip user ROM	2K	no	2K	no
On-chip timer	yes	yes	yes	yes
On-chip timer prescaler	yes	yes	yes	yes
Bidirectional ports/lines	3/24	3/24	3/24	3/24
Input-only port/lines	1/8	1/8	1/8	1/8
Analog on input lines (A/D)	yes	yes	no	no

1-18. EMULATOR CONTROLLER.

1-19. The emulator pod cannot provide emulation unless it is connected to a Hewlett-Packard Model 64191A Emulator Controller. Because the 6805 R/U microcomputers have less than 4K bytes of on-chip memory, the emulator controller is able to provide all necessary emulation memory. No memory option cards are needed.

1-20. The controller passes instructions between the development station and the emulator pod. It also places emulator address, data and status on the emulation bus within the development station. Various option cards can be connected to the emulation bus to analyze the emulator operation.

1-21. ACCESSORIES SUPPLIED.

1-22. An RFI ground bracket is supplied with the Model 64192A 6805 R/U Emulator Pod to ground the shielded emulator pod cable. See section II, installation.

1-23. ADDITIONAL EQUIPMENT REQUIRED.

1-24. The Model 64192A 6805 R/U Emulator Pod must be connected to a Model 64191A 6805 Emulator Controller that is installed in a Hewlett-Packard 64000 series development station.

1-25. POWER REQUIREMENTS.

1-26. Power requirements of the 6805 R/U emulator subsystem are shown in the table 1-3. Maximum power useage is 13.5 watts, with typical operation at 11.5 watts.

Table 1-3. Power Supply Loads

Supply	+5 V
Pod current	1.1 A
Controller current	1.2 A
Total	2.3 A

1-27. CONVENTIONS.

1-28. The following conventions are used in the text and schematics.

a. Abbreviations, see table 6-1.

b. Mnemonics (signal names); see table 8-2.

c. Logic symbols, see table 8-3.

d. Softkeys are indicated by arrow brackets, while normal keys are shown in square brackets. For example, <stop> indicates the software labeled stop key, while [RETURN] indicates the keyboard labeled return key.

e. Component designators are assigned according to the numbered-row, lettered-column method for integrated circuit packages. Discrete components are assigned reference designators using the upper left to lower right method.

f. TTL logic levels (in volts):

Input high threshold	Input low threshold	Output high threshold	Output low threshold
+2.0	+0.8	+2.4	+0.2

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information necessary to install the Model 64192A 6805 R/U Emulator Pod in the Model 64000 Logic Development System. Also included is information concerning initial inspection, damage claims, environmental considerations, storage and shipment.

2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until contents have been checked for completeness and the model 64191A has been checked mechanically and electrically. If the contents are incomplete, if there is mechanical damage or defect, or if the model 64192A does not pass performance verification, notify the nearest Hewlett-Packard office. If the shipping container or cushioning material is damaged, notify the carrier as well as the Hewlett-Packard office. Keep the shipping materials for carrier's inspection. The Hewlett-Packard office will arrange for repair or replacement at HP option without waiting for claim settlement.

2-5. DEVELOPMENT STATION CONFIGURATION.

2-6. The controller should be installed in the highest numbered slot of the development station. When a logic analyzer option card is used with the emulator, the analyzer should be installed in the next lower numbered slot adjacent to the emulator control board. See figure 2-1.

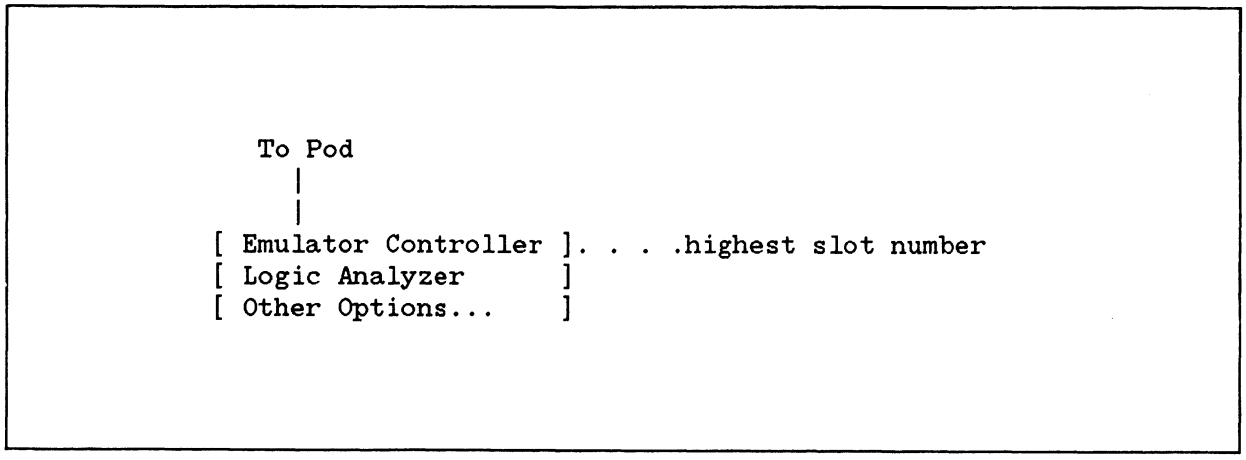


Figure 2-1. Development Station Card Cage

CAUTION

Before installing the emulator subsystem, read the safety summary at the front of the manual.

CAUTION

The following precautions should be taken while using Hewlett-Packard emulator pods. Damage to the emulator circuitry may result if these precautions are not observed.

⚠ TURN OFF THE POWER. Turn off power to the user target system and the emulation development station, before inserting the user plug, to avoid circuit damage resulting from voltage transients or mis-insertion of the user plug.

⚠ VERIFY USER PLUG ORIENTATION. Make certain that pin 1 of the target system microprocessor socket, and pin 1 of the user plug, are properly aligned before inserting the user plug into the socket. Failure to do so may result in damage to the emulator circuitry.

⚠ PROTECT AGAINST STATIC DISCHARGE. The emulator pod contains devices which are susceptible to damage by static discharge. Therefore, operators should take precautionary measures before handling the user plug to avoid emulator damage.

⚠ CONNECT THE RFI GROUND BRACKET. The emulator controller and pod can be damaged by static discharge when the emulator pod cable is not firmly clamped in place.

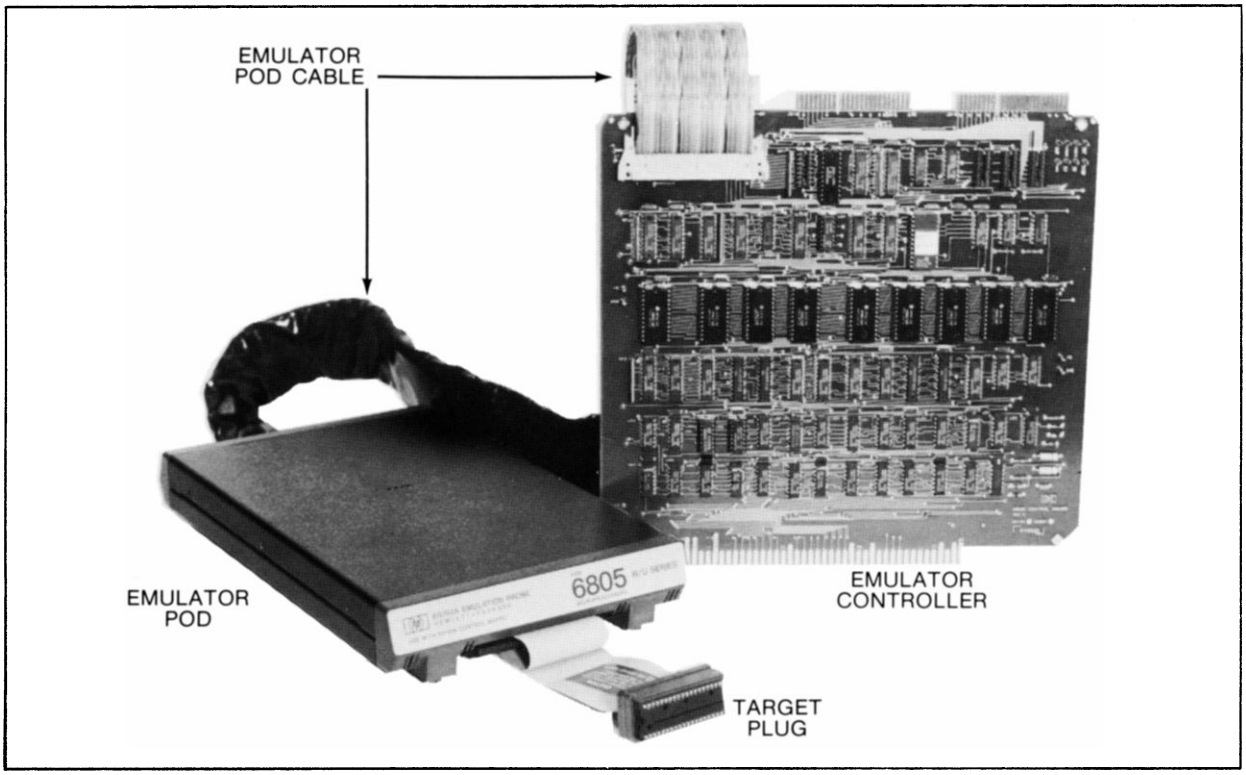


Figure 2-2. 6805 R/U Emulator Subsystem

2-7. INSTALLATION.

2-8. To install the emulator controller and pod proceed as follows:

a. Remove the card cage cover. Position the development station so there is clear access to the card cage.

b. Before placing the controller into the card cage, connect the emulator pod to it as directed in steps c and d.

c. Locate the two multi-colored ribbon cables within the emulator pod cable. One ribbon cable is terminated in a female card-edge connector; the other is terminated in a female socket type connector. Locate pin 1, it is indicated by a triangle molded into the connector.

d. Locate the mating male connectors on the controller. They are at the top left of the board, as you face the component side, and have color dots that match dots on the cables. Pin 1 of the male connectors is etched on the board. Align the connectors and attach the cables to the controller.

e. Next, insert the controller into the highest numbered slot. Insure that it is completely seated in the motherboard.

f. Refer to figure 2-3. If the development station has an RFI ground bracket/clamp bar as shown in the figure, perform the next step. If it does not have an RFI ground bracket/clamp bar, attach the bracket/bar as directed on the following page before going to step 'g'.

g. Loosen the clamp bar and slip the emulator pod cable beneath it, placing the wire mesh is directly beneath the bar. Tighten the clamp bar to hold the cable firmly in place.

h. If a logic analyzer option card is to be connected, refer to the appropriate manual and connect it to the control board now.

i. Carefully fold all cables over the boards so as not to damage them. Replace the card cage cover.

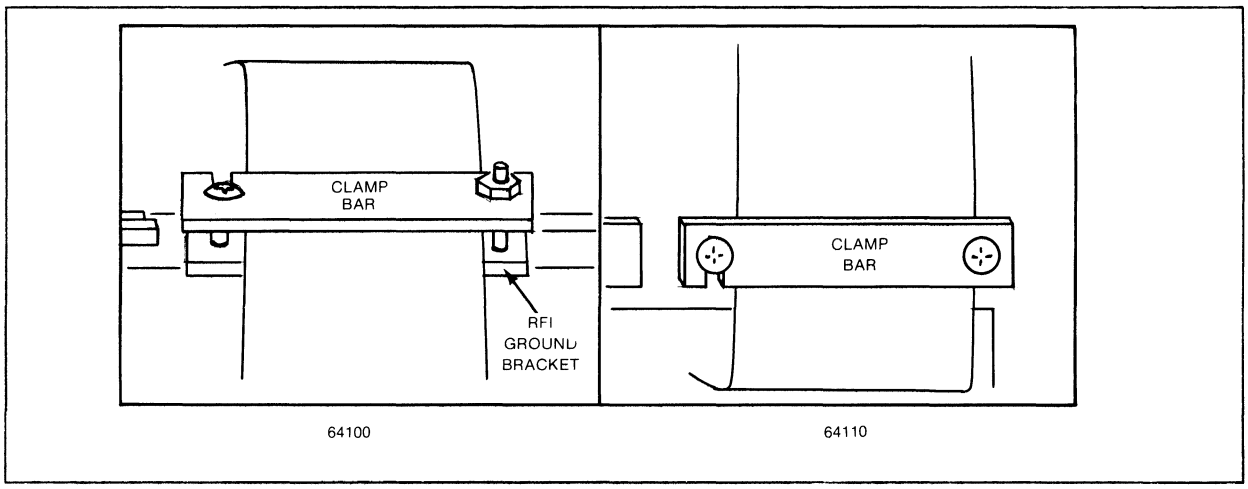


Figure 2-3. RFI Ground Bracket/Clamp Bar

2-9. REMOVAL.

2-10. To remove the controller and pod proceed as follows:

a. Remove the card cage cover. Position the development station so there is clear access to the card cage.

b. If a logic analyzer option card is connected to the controller, disconnect it.

c. Loosen the RFI ground bracket clamp bar and slip the emulator pod cable from beneath it.

d. Next, Remove the controller from the card cage slot.

e. Replace the card cage cover.

2-11. RFI GROUND BRACKET INSTALLATION.

2-12. The emulator pod is shipped with a plastic bag that contains an RFI ground bracket assembly. The assembly includes an RFI ground bracket, clamp bar and miscellaneous hardware. These parts are used in the steps shown below.

2-13. MODEL 64100A DEVELOPMENT STATION.

a. Position the development station so there is clear access to the back.

b. Facing the back, remove the right cable clamp; it is secured by two #6-32 screws along the top edge. Discard these screws.

c. Replace the old cable clamp with the RFI ground bracket, and attach with two new #6-32 x .375 long pan head screws, through the back of the card cage.

d. Locate the clamp bar and position it with the oblong hole over the threaded stud.

e. Install the #6-32 hex nut on the threaded stud, and install the #6-32 x 1.000 long pan head screw in the threaded hole along the top edge of the card cage.

2-14. MODEL 64110A DEVELOPMENT STATION.

a. Position the development station so there is clear access to the back.

b. Facing the back, remove the right cable clamp bracket; it is secured by two #4-40 screws. Discard these screws.

c. Place a number 4 washer on each #4-40 x .750 pan head screw and insert one screw with washer through the oblong hole in the clamp bar. Then mount the clamp bar with the two #4-40 x .750 long pan head screws where the old cable clamp bracket had been.

2-15. OPERATING ENVIRONMENT.

2-16. The Model 64192A 6805 R/U Emulator Pod can be operated in environments within the limits shown below. It should be protected from temperature extremes which cause condensation within the instrument.

Temperature.....0 to +40 degrees Celsius.
Humidity.....5 to 80 % relative humidity.
Altitude.....4,600 m (15,000 ft).

2-17. STORAGE AND SHIPPING ENVIRONMENT.

2-18. The Model 64192A 6805 R/U Emulator Pod can be stored and shipped in environments within the limits given below.

Temperature.....-40 to +40 degrees Celsius.
Humidity.....5 to 80 % relative humidity.
Altitude.....15,240 m (50,000 ft).

2-19. ORIGINAL PACKAGING.

2-20. Containers and packing materials identical to those used in factory packaging are available through Hewlett-Packard sales and service offices.

2-21. OTHER PACKAGING.

2-22. The following general instructions should be used for repackaging with commercially available materials.

a. Wrap the Model 64192A 6805 R/U Emulator Pod in heavy paper or plastic. Use a strong shipping container. A double wall carton made of 350 pound test material is adequate.

b. Use a layer of shock absorbing material 70 to 100 mm (3 to 4 inch) thick around all sides of the model 64192A to provide firm cushioning and prevent movement inside the container

c. Seal shipping container securely.

d. Mark shipping container FRAGILE to request careful handling.

e. In any correspondence, refer to instrument by model number and full repair number.

SECTION III

OPERATION

3-1. INTRODUCTION.

3-2. This section contains a brief description of the 6805 R/U emulator functions that are selected by the user. Complete operation from the development station keyboard is beyond the scope of this service manual. Please refer to the operator's manuals for the procedures.

3-3. 6805 R/U MICROCOMPUTER CONFIGURATION.

3-4. Before running the emulator, the user must chose a microcomputer configuration. Table 3-1 shows the choices available on the development station display. The following items are configuration choices that are related to the 6805 emulator subsystem hardware.

3-5. Clock Source. The user can choose a 4 MHz crystal located on the emulator pod upper board, or an external clock located on the target system. The choice is affected by hardware on the emulator pod upper board.

3-6. Restrict To Real-Time Runs. This is a feature controlled by software that prevents the user from selecting operations that interrupt the emulator processor during user program emulation.

3-7. Break On Illegal Opcodes. The emulator can be stopped when an illegal opcode is detected, if the user selects this option. Break circuitry is located on the emulator controller.

3-8. Break On Write To ROM. An illegal write to the ROM area of memory can be detected and cause the emulator to stop, if this option is selected by the user. Break circuitry is located on the emulator controller.

3-9. Microprocessor To Be Emulated. One of four different 6805 R/U microcomputers can be selected. Circuitry on the emulator controller and the emulator pod implement the choice of MC6805R2, MC6805R3, MC6805U2, or MC6805U3.

3-10. Timer Mode. When the MC6805R3 or MC6805U3 are chosen, the choice of timer mode is required. The mode can be mask-option or software. The choice of mask-option means that the register in EPROM known as the Mask Option Register (MOR) is selected to control the timer. When software is selected, the Timer Control Register (TCR) is chosen to control the timer. The TCR is loaded by user software. The choice is affected by circuitry on the emulator pod lower board.

3-11. Timer Source. Choice of the MC6805R2 or MC6805U2 allows only a choice of internal-gated or external timer source. When the R3 or U3 timer mode is software, the timer source can be off, internal, internal-gated, or external. These choices are implemented in circuitry on the emulator pod lower board.

3-12. Timer Prescaler. On all four microcomputers, a timer prescaler factor must be chosen. One of the eight possible scaling values is affected in hardware located on the emulator pod lower board.

3-13. Modify Simulated I/O. This software feature does not affect the emulator hardware. See operating manual for details.

3-14. Modify Interactive Measurement System. The emulator hardware is not effected by this software feature. See operating manual for details.

Table 3-1. 6805 R/U Microcomputer Configuration

```
< >  Micro-processor clock source?
     internal  external

< >  Restrict to real-time runs?
     yes  no

< >  Break processor on illegal opcodes?
     yes  no

< >  Break processor on write to ROM?
     yes  no

< >  Microprocessor to be emulated:
     MC6805R2  MC6805R3  MC6805U2  MC6805U3

< >  Timer mode:
     mask_opt  software

< >  Timer source:
     off  internal  internal_gated  external

< >  Prescale:
     1  2  4  8  16  32  64  128

< >  Modify simulated I/O?
     yes  no

< >  Modify interactive measurement specification?
     yes  no
```

SECTION IV

PERFORMANCE TESTS

4-1. INTRODUCTION.

4-2. This section describes the performance verification (PV) for the 6805 R/U emulator subsystem. Both the Model 64191A 6805 Emulator Controller and the Model 64192A 6805 R/U Emulator Pod are tested by these procedures.

4-3. SYSTEM CONSIDERATIONS.

4-4. Failure isolation must be performed to eliminate other sections of the logic development system as the source of the failure. It is assumed in this manual that the development station PV has been successfully conducted and that other option cards have also been checked. It is also assumed that the target system being emulated has been disconnected from the emulator pod, thus eliminating it as a possible source of the failure.

4-5. PERFORMANCE VERIFICATION TESTS.

4-6. The performance verification for the 6805 R/U emulator subsystem is a subsection of the system Option Test Performance Verification. The system-level-PV tests all option modules that are located in the development station card cage. The following paragraphs describe how to perform the 6805 R/U emulator subsystem PV and what is checked.

4-7. REQUIRED EQUIPMENT.

a. Development station with most recent PV software. Stations operating from local flexible disc must have the software modules shown below. Other software modules may be required, such analysis software to perform analysis stimulus tests.

FLOPPY_OP_SYS	OPTION_TEST	pv_6805:HP

b. To test internal analysis, an internal analysis option card must be present and connected to the emulator controller.

c. To print PV results, a printer must be attached to the system.

4-8. STARTING PERFORMANCE VERIFICATION.

4-9. To test the 6805 R/U emulator subsystem, proceed as follows.

a. With the operating system initialized and awaiting a command, figure 4-1, enter:

option_test [RETURN]

b. The PV now displays a directory of the installed option boards and their card slot numbers, figure 4-2. The first step in the PV is to locate the card slot of the Model 64191A 6805 Emulator Controller and enter the slot number. For example, if the emulator controller is in slot 8 of the card cage, enter:

8 [RETURN]

c. When one or no analysis option card is present, the next display is the Total PV display. When more than one analysis option card is in the card cage, the display requests choice of analysis card slot, or no card. Enter the slot number of the analysis card that is connected to the 6805 emulator controller. The next display is the Total PV.

4-10. PERFORMANCE VERIFICATION COMMANDS.

4-11. Each PV display provides prompting for commands that can be executed. These commands are selected by 'softkeys' that are defined in table 4-1.

Table 4-1. Performance Verification Softkeys

<cycle>	starts highlighted test and continues through other tests. When pressed during cycling, it stops the testing.
<disp_test>	displays test details.
<end>	terminates performance verification and returns to the card cage directory display. It resets all test and failure counters to zero.
<exit_test>	stops the test and returns to next higher level display.
<next_test>	moves highlight line to following test category.
<print>	outputs display to attached printer.
<start>	begins the test. When pressed during testing, it stops the test.

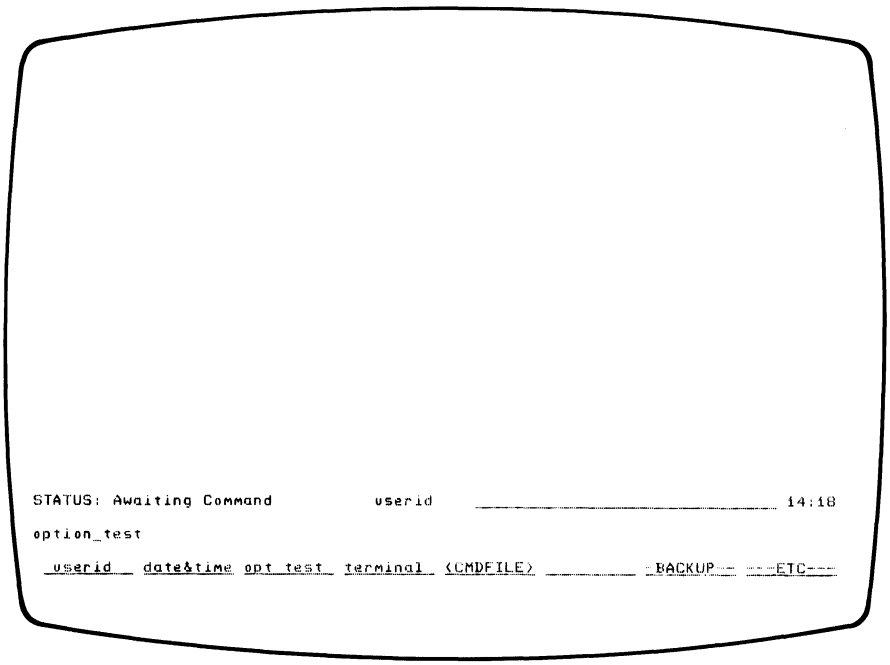


Figure 4-1. System Awaiting Command Display

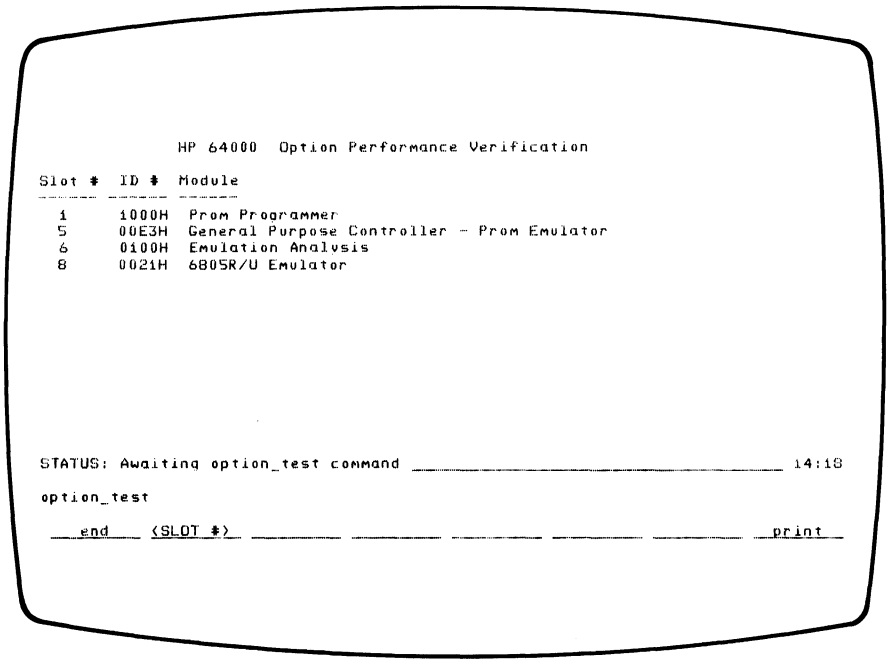


Figure 4-2. Card Cage Directory Display

4-12. TOTAL PV DISPLAY.

4-13. Purpose. All test categories available for the card cage configuration are shown in this display. When one or more test categories have been executed, the results are displayed. Use the display to choose the test categories to be performed or to review the overall results of the PV.

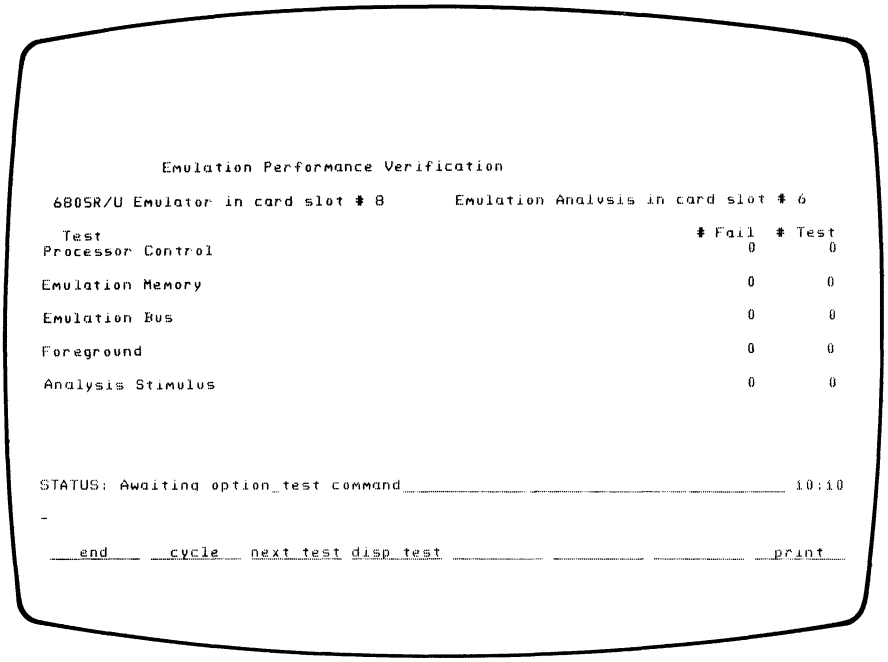


Figure 4-3. Total PV Test Display

4-14. Running the Total PV. To run all the tests shown on the display, press the <cycle> softkey. Each test category is executed and the results are displayed. A complete cycle requires approximately 5 seconds. To stop the iterations, press the <cycle> softkey again.

4-15. Using the Total PV Results. When the tests are complete, examine the # Fail column. When all entries are zero, it indicates the percentage of circuit nodes shown below have been checked and no errors have been found. Note that microcomputer port D is not tested.

Controller 90% Pod, upper board 84% Pod, lower board 63%

4-16. A non-zero value represents the number of errors detected in the test category. Determine the exact cause of the error by viewing the failed test category in detail. Do this by positioning the highlight line over the test category and pressing the <disp_test> softkey.

4-17. PROCESSOR CONTROL TEST DISPLAY.

4-18. Purpose. The three tests shown on this display check basic features of the emulator controller and pod. When these tests fail, the results of further tests are not necessarily valid.

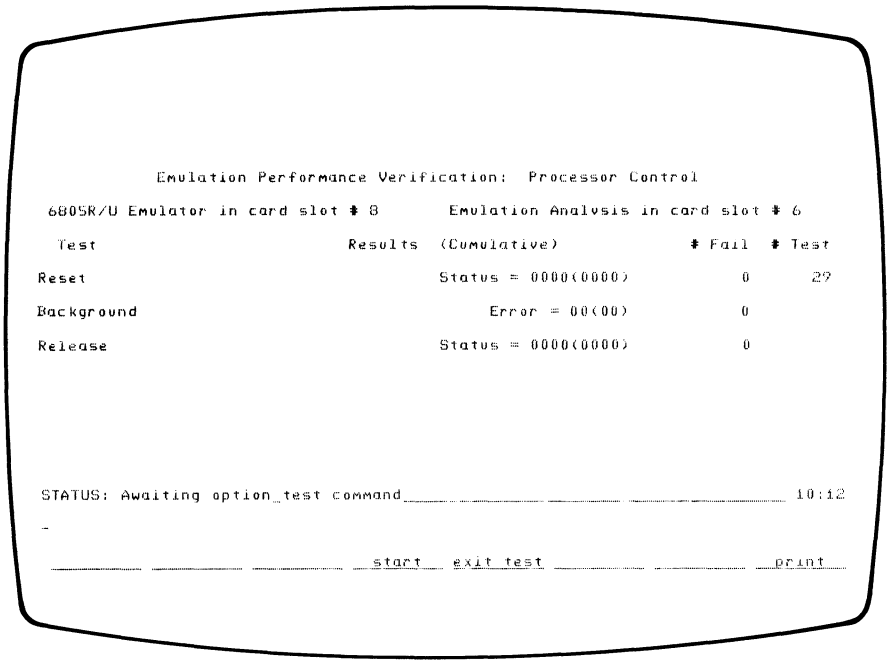


Figure 4-4. Processor Control Test Display

4-19. Running the Processor Control Test. To view this test display, begin with the Total PV Display (figure 4-3). Position the highlight line over 'Processor Control' and then press the <disp_test> softkey. Next, press the <start> softkey, the test begins immediately and continues to run until a softkey is pressed. Each iteration takes less than one second.

4-20. Using the Processor Control Results. The # Fail column shows the total number of errors detected during the test. Each error code in the results column represents a single failure encountered during the last iteration. The cumulative error code in parenthesis represents the sum of all errors detected during the test. Cumulative error codes that differ from error codes in the results column indicate multiple, or intermittent errors. When the error codes are the same, the errors are systematic.

4-21. PROCESSOR CONTROL, RESET.

4-22. How. The development station selects the emulator and clears all break bits; it waits, then reads the emulator status bits. The status bits are compared to expected values and any discrepencies are noted in the display.

4-23. Results. Errors found in this test are due to failures in the emulator controller. Results of succeeding tests are not necessarily valid when this test fails. Error bits are decoded as follows:

	Bits	Status Bit in Error
Status = 0000(0000)	0000	None
	---1	Slow clock
	--1-	Background
	-1--	Illegal opcode
	1---	Illegal memory reference

4-24. PROCESSOR CONTROL, BACKGROUND.

4-25. How. The development station directly writes a walking 1 data pattern to each background memory address. The data at each background memory address is read, compared with the expected pattern, and written with a walking 0 pattern. Then, each location is read, compared with the expected pattern. Any discrepencies are displayed as bad bits.

4-26. Results. Errors found in this test are due to failures in the emulator controller. Results of succeeding tests are not necessarily valid when this test fails. The hexidecimal error word is decoded as follows:

	Hex	Binary	Signal in error
Error = 00(00)	xx =	0000 0000	None
		---- ---1	LED0
		---- --1-	LED1
		---- -1--	LED2
		---- 1---	LED3
		---1 ----	LED4
		--1- ----	LED5
		-1-- ----	LED6
		1--- ----	LED7

4-27. PROCESSOR CONTROL, RELEASE.

4-28. How. The development station loads background memory with a test program for the emulator processor to execute. After waiting, the mainframe instructs the emulator processor to read its trap address and stack pointer. Any discrepencies from expected values are noted as errors in the # Fail column. No decoding of these errors is possible.

4-29. The emulator status bits are then read, compared to expected values, and the errors codes are displayed.

4-30. Results. Errors found in this test are due to failures in either the emulator controller or pod. Results of succeeding tests are not necessarily valid when this test fails. Error bits are decoded as follows:

	Bits	Status Bit in Error
Status = 0000(0000)	0000	None
	---1	Slow clock
	--1-	Background
	-1--	Illegal opcode
	1---	Illegal memory reference

4-31. EMULATION MEMORY TEST DISPLAY.

4-32. Purpose. The four tests shown on this display check the ability of the development station to directly access all 8 K of emulation foreground memory.

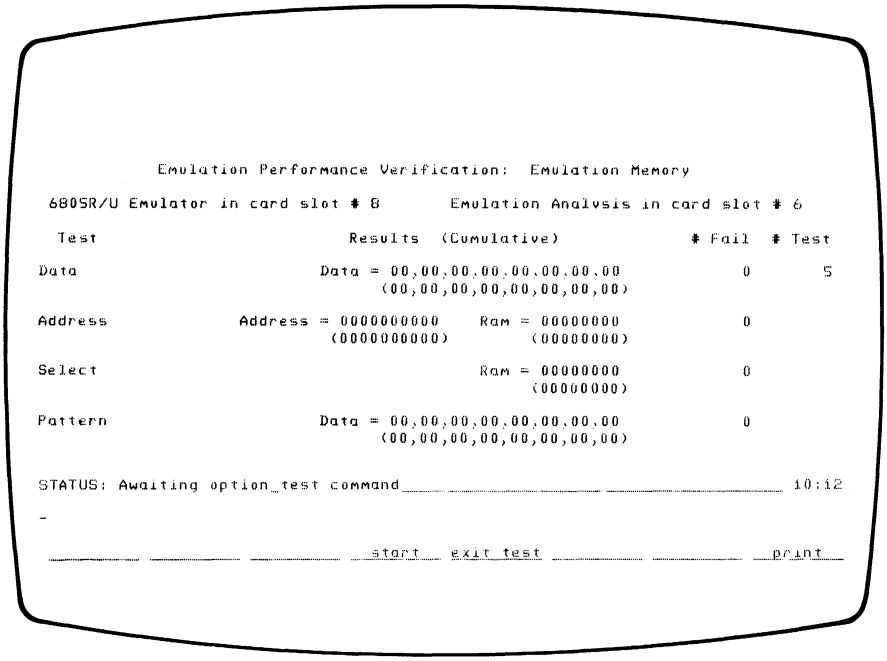


Figure 4-5. Emulation Memory Test Display

4-33. Running the Emulation Memory Test. To view this test display, begin with the Total PV Display (figure 4-3). Position the highlight line over 'Emulation Memory' and then press the <disp_test> softkey. Next, press the <start> softkey, the test begins immediately and continues to run until a softkey is pressed. Each iteration takes less than one second.

4-34. Using the Emulation Memory Results. The # Fail column shows the total number of errors detected during the test. Each error code in the results column represents a single failure encountered during the last iteration. The cumulative error code in parenthesis represents the sum of all errors detected during the test. Cumulative error codes that differ from error codes in the results column indicate multiple, or intermittent errors. When the error codes are the same, the errors are systematic.

4-35. EMULATION MEMORY, DATA.

4-36. How. The development station selects the emulator and clears all break bits. The first address of each the eight foreground RAMs is tested with walking 1 and 0 data patterns. Any discrepencies from expected data patterns are displayed as bad bits.

4-37. Results. Errors found in this test are due to failures in the emulator controller. Results of succeeding tests are not necessarily valid when this test fails. The hexidecimal error words are decoded as follows:

	Hex	Binary	Signal in error
Data = 00, 00, 00, 00, 00, 00, 00, 00	xx	= 0000 0000	None
(00, 00, 00, 00, 00, 00, 00, 00)		---- ---1	LED0
		---- --1-	LED1
RAM U3H U3A U3I U3C U3K U3D U3L U3F		---- -1--	LED2
		---- 1---	LED3
		---1 ----	LED4
		--1- ----	LED5
		-1-- ----	LED6
		1--- ----	LED7

4-38. EMULATION MEMORY, ADDRESS.

4-39. How. The development station directly accesses each RAM in foreground memory. Selected addresses are tested by writing and reading complementary bit patterns. Any descrepencies with expected values are noted as errors in the display.

4-40. Results. Errors found in this test are due to failures in the emulator controller. Results of succeeding tests are not necessarily valid when this test fails. The error bits are decoded as follows:

a. Address = 0000000000
(0000000000)

Bits	Signal in error
0000000000	None
---------1	LEA0
--------1-	LEA1
-------1--	LEA2
------1---	LEA3
-----1----	LEA4
----1-----	LEA5
---1------	LEA6
--1-------	LEA7
-1--------	LEA8
1---------	LEA9

b. RAM = 00000000
(00000000)

Bits	RAM in error
00000000	None
-------1	U3F
------1-	U3L
-----1--	U3D
----1---	U3K
---1----	U3C
--1-----	U3I
-1------	U3A
1-------	U3H

4-41. EMULATION MEMORY, SELECT.

4-42. How. The development station directly accesses each RAM in foreground memory. It writes a pattern to address zero of the RAM under test and then writes the complement of the pattern to address zero of the other RAMs. The data is read back and any descrepencies from expected values is flagged as an error in the display.

4-43. Results. Errors found in this test are due to failures in the emulator controller. Results of succeeding tests are not necessarily valid when this test fails. The error bits are decoded as follows:

	Bits	RAM in error
Ram = 00000000	00000000	None
(00000000)	-------1	U3F
	------1-	U3L
	-----1--	U3D
	----1---	U3K
	---1----	U3C
	--1-----	U3I
	-1------	U3A
	1-------	U3H

4-44. EMULATION MEMORY, PATTERN.

4-45. How. The development station directly writes a random pattern to each address of each RAM in foreground memory. It then reads all addresses, writes the complement of the pattern, then reads all address again. Any deviation from expected values are noted as errors in the display.

4-46. Results. Errors found in this test are due to failures in the emulator controller. Results of succeeding tests are not necessarily valid when this test fails. The hexidecimal error words are decoded as follows:

		Hex	Binary	Signal in error
Data = 00, 00, 00, 00, 00, 00, 00, 00		xx	= 0000 0000	None
(00, 00, 00, 00, 00, 00, 00, 00)			---- ---1	LED0
			---- --1-	LED1
RAM U3H U3A U3I U3C U3K U3D U3L U3F			---- -1--	LED2
			---- 1---	LED3
			---1 ----	LED4
			--1- ----	LED5
			-1-- ----	LED6
			1--- ----	LED7

4-47. EMULATION BUS TEST DISPLAY.

4-48. Purpose. The four tests shown on this display check the ability of the emulator processor to correctly access foreground memory. Only memory up to the maximum address for the emulator is tested.

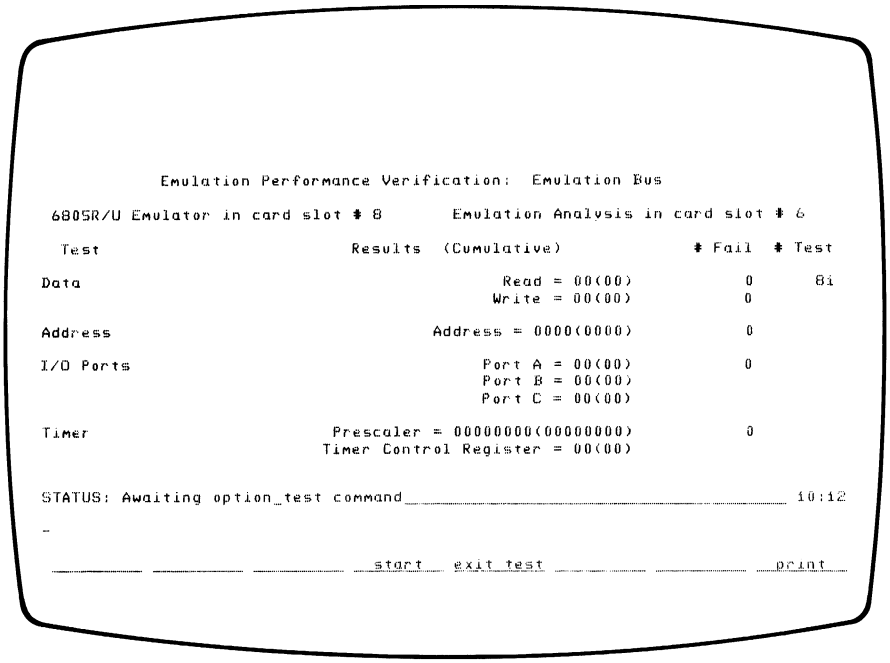


Figure 4-6. Emulation Bus Test Display

4-49. Running the Emulation Bus Test. To view this test display, begin with the Total PV Display (figure 4-3). Position the highlight line over 'Emulation Bus' and then press the <disp_test> softkey. Next, press the <start> softkey, the test begins immediately and continues to run until a softkey is pressed. Each iteration takes less than one second.

4-50. Using the Emulation Bus Results. The # Fail column shows the total number of errors detected during the test. Each error code in the results column represents a single failure encountered during the last iteration. The cumulative error code in parenthesis represents the sum of all errors detected during the test. Cumulative error codes that differ from error codes in the results column indicate multiple, or intermittent errors. When the error codes are the same, the errors are systematic.

4-51. EMULATION BUS, DATA.

4-xx. How. The development station selects the emulator and loads background memory with a test program. Address 0080H through the highest address for the emulator are tested with walking 1 and 0 patterns. First, the mainframe directly writes to the memory then the emulator reads it. Next, the emulator processor writes to the emulation memory and the mainframe directly reads it. Any descrepencies are flagged as errors in the display.

4-52. Results. Errors found in this test are due to failures in the emulator controller or pod. Results of succeeding tests are not necessarily valid when this test fails. The hexidecimal error words are decoded as follows:

a. Read = 00(00)

Hex	Binary	Signal in error
xx =	0000 0000	None
	---- ---1	LED0
	---- --1-	LED1
	---- -1--	LED2
	---- 1---	LED3
	---1 ----	LED4
	--1- ----	LED5
	-1-- ----	LED6
	1--- ----	LED7

b. Write = 00(00)

Hex	Binary	Signal in error
xx =	0000 0000	None
	---- ---1	LED0
	---- --1-	LED1
	---- -1--	LED2
	---- 1---	LED3
	---1 ----	LED4
	--1- ----	LED5
	-1-- ----	LED6
	1--- ----	LED7

4-53. EMULATION BUS, ADDRESS.

4-54. How. Selected addresses from 0080H through the highest address for the emulator are tested with walking 1 and 0 patterns. First, the development station directly writes to the memory then the emulator reads it. Next, the emulator processor writes to the emulation memory and the mainframe directly reads it. Any discrepencies are flagged as errors in the display.

4-55. Results. Errors found in this test are due to failures in the emulator controller or pod. Results of succeeding tests are not necessarily valid when this test fails. The hexidecimal error words are decoded as follows:

	Hex	Binary	Signal in error
Address = 0000(0000)	xxxx =	0000 0000 0000 0000	None
		---- ---- ---- ---1	LEA0
		---- ---- ---- --1-	LEA1
		---- ---- ---- -1--	LEA2
		---- ---- ---- 1---	LEA3
		---- ---- ---1 ----	LEA4
		---- ---- --1- ----	LEA5
		---- ---- -1-- ----	LEA6
		---- ---- 1--- ----	LEA7
		---- ---1 ---- ----	LEA8
		---- --1- ---- ----	LEA9
		---- -1-- ---- ----	LEA10
		---- 1--- ---- ----	LEA11
		---1 ---- ---- ----	LEA12
		--1- ---- ---- ----	LEA13
		-1-- ---- ---- ----	LEA14
		1--- ---- ---- ----	LEA15

4-57. EMULATION BUS, I/O PORTS.

4-58. How. The emulator processor sets the data-direction registers for ports A, B, and C to be output ports. A series of walking 1 and 0 patterns are written to the ports. The port bits are read and compared to expected values. Any discrepencies are noted as errors in the display.

NOTE

Microcomputer port D is not tested.

4-59. Results. Errors found in this test are due to failures in the emulator controller or pod. Results of succeeding tests are not necessarily valid when this test fails. The hexidecimal error words are decoded as follows:

	Hex	Binary	Port bit in error
Port A = 00(00) Port B = 00(00) Port C = 00(00)	xx =	0000 0000	None
		---- ---1	0
		---- --1-	1
		---- -1--	2
		---- 1---	3
		---1 ----	4
		--1- ----	5
		-1-- ----	6
		1--- ----	7

4-60. EMULATION BUS, TIMER.

4-61. How. The development station selects the emulator, loads test programs into foreground and background memory, initializes the pod option register, and clears the timer prescaler. The timer is tested for each prescaler value by setting the timer to a known value and then stepping the emulator to decrement the counter. The timer is read and compared to expected values. Any errors are displayed as failing prescaler bits.

4-62. The timer control register is tested by writing a walking 1 and 0 pattern and checking the results against expected values.

4-63. Results. Errors found in this test are due to failures in the emulator controller or pod. Results of succeeding tests are not necessarily valid when this test fails. The errors are decoded as follows:

	Bits	Prescaler bit in error
Prescaler = 00000000(00000000)	00000000	None
	-------1	0
	------1-	1
	-----1--	2
	----1---	3
	---1----	4
	--1-----	5
	-1------	6
	1-------	7

	Hex	Binary	Signal in error
Timer Control Register = 00(00)	xx =	0000 0000	None
		---- ---1	TCR0
		---- --1-	TCR1
		---- -1--	TCR2
		---- 1---	TCR3
		---1 ----	TCR4
		--1- ----	TCR5
		-1-- ----	TCR6
		1--- ----	TCR7

4-64. FOREGROUND TEST DISPLAY.

4-65. Purpose. The five tests shown on this display check the ability of the emulator processor to correctly run programs in foreground memory and to detect illegal opcodes.

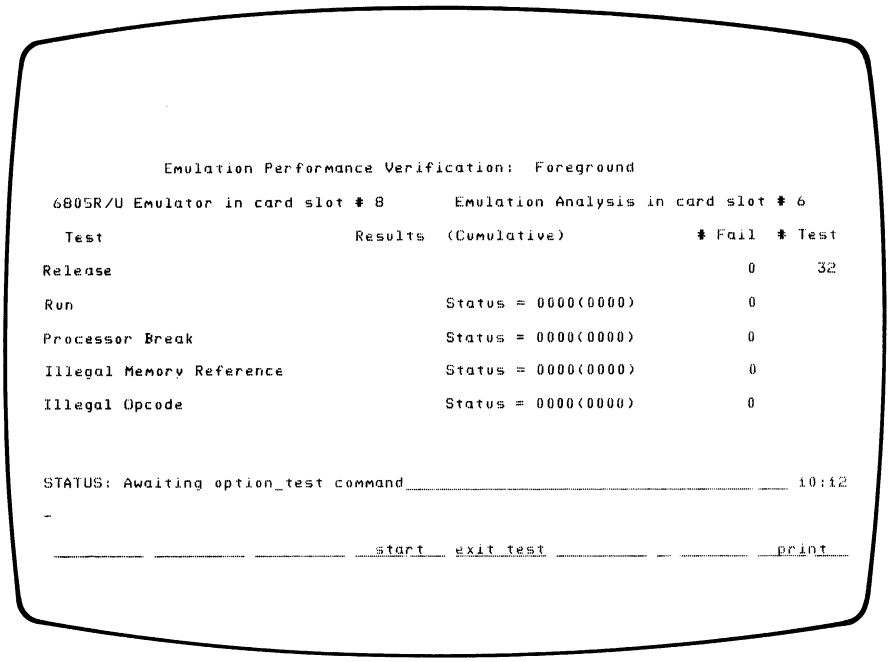


Figure 4-7. Foreground Test Display

4-66. Running the Foreground Test. To view this test display, begin with the Total PV Display (figure 4-3). Position the highlight line over 'Foreground' and then press the <disp_test> softkey. Next, press the <start> softkey, the test begins immediately and continues to run until the <end> softkey is pressed. Each iteration takes less than one second.

4-67. Using the Foreground Results. The # Fail column shows the total number of errors detected during the test. Each error code in the results column represents a single failure encountered during the last iteration. The cumulative error code in parenthesis represents the sum of all errors detected during the test. Cumulative error codes that differ from error codes in the results column indicate multiple, or intermittent errors. When the error codes are the same, the errors are systematic.

4-68. FOREGROUND, RELEASE.

4-69. How. The development station loads background memory with a test program for the emulator processor to execute. After waiting, the mainframe instructs the emulator processor to read its trap address and stack pointer. Any discrepencies from expected values are noted as errors in the # Fail column. No decoding of these errors is possible.

4-70. Results. Errors found in this test are due to failures in the emulator controller or pod. The errors cannot be decoded.

4-71. FOREGROUND, RUN.

4-72. How. The development station loads foreground memory with a test program and instructs the emulator processor to run from address 0080H. After waiting, the development station reads the emulator status register and compares the status bits to expected values. Discrepencies are flagged as errors in the display.

4-73. Next, the emulator break line is set and selected foreground memory locations are checked to verify that the emulator ran the program and changed the data. Addresses that are mapped as user memory are checked to make certain the emulator did not alter the data. Any discrepencies are noted as errors in the # Fail column, but they cannot be decoded.

4-74. Results. Errors are decoded as follows:

	Bits	Status Bit in Error
Status = 0000(0000)	0000	None
	---1	Slow clock
	--1-	Background
	-1--	Illegal opcode
	1---	Illegal memory reference

4-75. FOREGROUND, PROCESSOR BREAK.

4-76. How. After the development station issues the emulator break command in the Run test, the emulator stack pointer is read and compared to expected values. Any discrepency is noted as an error in the # Fail column. No decoding of the error is possible. The emulator status register is also read after the break and compared to expected status. Discrepencies are flagged as errors in the display.

4-77. Results. Errors found in this test are due to failures in the emulator controller or pod. Results of succeeding tests are not necessarily valid when this test fails. Error bits are decoded as follows:

	Bits	Status Bit in Error
Status = 0000(0000)	0000	None
	---1	Slow clock
	--1-	Background
	-1--	Illegal opcode
	1---	Illegal memory reference

4-78. FOREGROUND, ILLEGAL MEMORY REFERENCE.

4-79. How. Four memory access tests are run to generate this error display. First, the development station selects the emulator and loads a test program into background memory.

4-80. Illegal Jump to Guarded Memory. The emulator is instructed to jump to a guarded-memory address. After waiting, the development station reads the last-address register and compares the address to the expected value. Any discrepency is noted as an error in the # Fail column. No decoding of the error is possible. The development station then reads the emulator status register and compares the status bits to expected values. Any discrepencies are noted as errors in the display.

4-81. Illegal Read From Guarded Memory. The emulator is instructed to read a guarded-memory address. After waiting, the development station reads the last-address register and compares the address to the expected value. Any discrepency is noted as an error in the # Fail column. No decoding of the error is possible. The development station then reads the emulator status register and compares the status bits to expected values. Any discrepencies are noted as errors in the display.

4-82. Illegal Write To ROM. The emulator is instructed to write to a ROM address. After waiting, the development station reads the lastaddress register and compares the address to the expected value. Any discrepency is noted as an error in the # Fail column. No decoding of the error is possible. The development station then reads the emulator status register and compares the status bits to expected values. Any discrepencies are noted as errors in the display.

4-83. Legal Write To ROM. The break on write to ROM bit is cleared and the emulator is instructed to write to ROM. After waiting, the development station reads the ROM address written to and compares the data to the expected value. Any discrepency is noted as an error in the # Fail column. No decoding of the error is possible.

4-84. The emulator status register is then read and compared with expected values. Any discrepencies are noted as error bits in the display.

4-85. Results. Errors found in this test are due to failures in the emulator controller or pod. Results of succeeding tests are not necessarily valid when this test fails. Error bits are decoded as follows:

	Bits	Status Bit in Error
Status = 0000(0000)	0000	None
	---1	Slow clock
	--1-	Background
	-1--	Illegal opcode
	1---	Illegal memory reference

4-86. FOREGROUND, ILLEGAL OPCODE.

4-87. How. The development station loads background memory with a test program, clears the break on illegal memory access bits, and loads a test program to foreground memory. The emulator processor is instructed to run the program that uses illegal opcodes. After waiting, the development station reads the last-opcode-address register and compares the data with expected values. Any discrepency is flagged as an error in the # Fail column. No decoding of the errors is possible.

4-88. The emulator status register is then read and compared with expected values. Any discrepencies are noted in the display. This process is repeated until all illegal opcodes have been tested.

4-89. Results. Errors found in this test are due to failures in the emulator controller or pod. Results of succeeding tests are not necessarily valid when this test fails. Error bits are decoded as follows:

	Bits	Status Bit in Error
Status = 0000(0000)	0000	None
	---1	Slow clock
	--1-	Background
	-1--	Illegal opcode
	1---	Illegal memory reference

4-90. ANALYSIS STIMULUS TEST DISPLAY.

4-91. Purpose. The five tests shown on this display check the interface between the 6805 emulator and an internal logic analyzer option card.

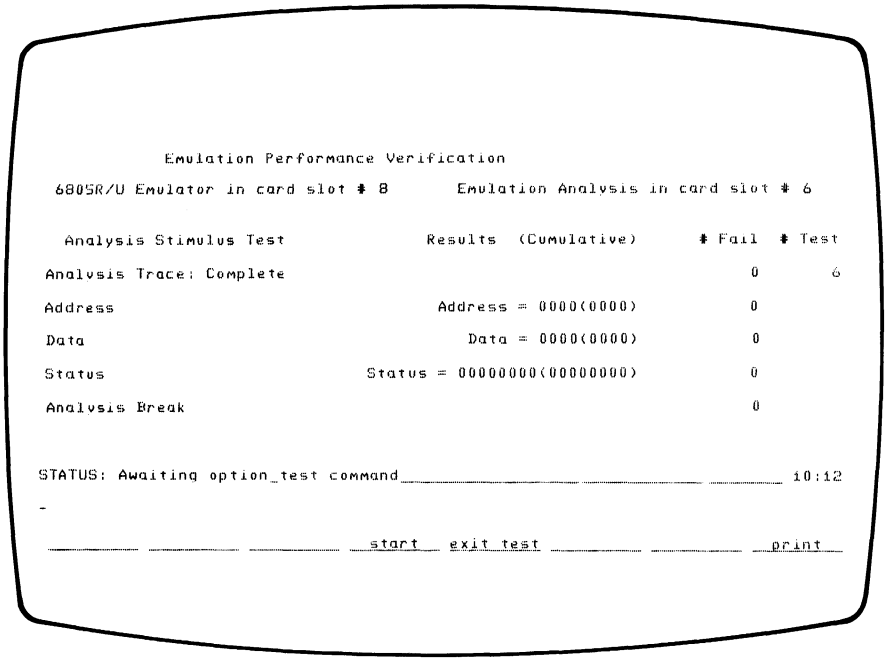


Figure 4-8. Analysis Stimulus Test Display

4-92. Running the Analysis Stimulus Test. To view this test display, begin with the Total PV Display (figure 4-3). Position the highlight line over 'Analysis Stimulus' and then press the <disp_test> softkey. Next, press the <start> softkey, the test begins immediately and continues to run until a softkey is pressed. Each iteration takes less than one second.

4-93. Using the Analysis Stimulus Results. The # Fail column shows the total number of errors detected during the test. Each error code in the results column represents a single failure encountered during the last iteration. The cumulative error code in parenthesis represents the sum of all errors detected during the test. Cumulative error codes that differ from error codes in the results column indicate multiple, or intermittent errors. When the error codes are the same, the errors are systematic.

4-94. ANALYSIS TRACE.

4-95. How. The development station selects the emulator and loads test programs into background and foreground memory. Next, the development station configures the analyzer to trace all emulation states and then releases both the emulator and analyzer to run. After waiting, the development station reads the analyzer measurement-complete bit. When the bit is false, the display indicates that the trace is not complete and further analysis tests are not run.

4-96. Results. Errors found in this test are due to failures in the emulator controller, internal analyzer, or connecting bus cables. The results are either trace complete, or trace incomplete.

4-97. ANALYSIS, ADDRESS.

4-98. How. When the analysis trace is successfully completed, the development station reads the analyzer memory and compares the address bits to expected values. Any discrepencies are displayed as bad bits.

4-99. Results. Errors found in this test are due to failures in the emulator controller, internal analyzer, or connecting bus cables. The hexidecimal error word is decoded as follows:

	Hex	Binary	Signal in error
Address = 0000(0000)	xxxx =	0000 0000 0000 0000	None
		---- ---- ---- ---1	LEA0
		---- ---- ---- --1-	LEA1
		---- ---- ---- -1--	LEA2
		---- ---- ---- 1---	LEA3
		---- ---- ---1 ----	LEA4
		---- ---- --1- ----	LEA5
		---- ---- -1-- ----	LEA6
		---- ---- 1--- ----	LEA7
		---- ---1 ---- ----	LEA8
		---- --1- ---- ----	LEA9
		---- -1-- ---- ----	LEA10
		---- 1--- ---- ----	LEA11
		---1 ---- ---- ----	LEA12
		--1- ---- ---- ----	LEA13
		-1-- ---- ---- ----	LEA14
		1--- ---- ---- ----	LEA15

4-100. ANALYSIS, DATA.

4-101. How. When the analysis trace is successfully completed, the development station reads the analyzer memory and compares the emulation data bits to expected values. Any discrepencies are displayed as bad bits.

4-102. Results. Errors found in this test are due to failures in the emulator controller, internal analyzer, or connecting bus cables. The hexidecimal error word is decoded as follows:

	Hex	Binary	Signal in error
Data = 00(00)	xx	= 0000 0000	None
		---- ---1	LED0
		---- --1-	LED1
		---- -1--	LED2
		---- 1---	LED3
		---1 ----	LED4
		--1- ----	LED5
		-1-- ----	LED6
		1--- ----	LED7

4-103. ANALYSIS, STATUS.

4-104. How. When the analysis trace is successfully completed, the development station reads the analyzer memory and compares the lowest four analyzer status bits to expected values. Any discrepencies in these bits are displayed as errors.

4-105. Results. Errors found in this test are due to failures in the emulator controller, internal analyzer, or connecting bus cables. The analyzer error bits are decoded as follows:

	Bits	Analyzer Status Bit in Error
Status = 0000(0000)	0000	None
	---1	0
	--1-	1
	-1--	2
	1---	3

4-106. ANALYSIS BREAK.

4-107. How. When the analysis trace is successfully completed, the development station reads the emulator status register on the emulator controller and compares the emulator status to expected values. Any discrepencies in these bits are displayed as errors.

4-108. Results. Errors found in this test are due to failures in the emulator controller, internal analyzer, or connecting bus cables. No decoding of errors is possible.

SECTION V

ADJUSTMENTS

There are no adjustments on the Model 64192A 6805 R/U Emulator Pod.

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering parts for the Model 64192A 6805 R/U Emulator Pod. Table 6-1 lists abbreviations used in the parts list and throughout the manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturers' five digit code numbers.

6-3. ABBREVIATIONS.

6-4. Table 6-1 lists abbreviations used in the parts list, the schematics and throughout the manual. In some cases, two forms of the abbreviation are used: one, all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lowercase and uppercase letters.

6-5. REPLACEABLE PARTS.

6-6. Table 6-2, the replaceable parts list, is organized as follows:

a. Chassis mounted parts in alphanumerical order by reference designator.

b. Electrical assemblies and their components in alphanumerical order by reference designator.

c. Miscellaneous parts.

6-7. The total quantity for each part is given only once, at the first appearance of the part number in the list. The information given for each part consists of the following.

a. The Hewlett-Packard part number and the check digit.

b. The total quantity (Qty) in the instrument.

c. The description of the part.

d. A five digit code that indicates the manufacturer.

e. The manufacturer's part number.

6-8. ORDERING INFORMATION.

6-9. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard office.

6-10. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument repair number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

6-11. DIRECT MAIL ORDER SYSTEM.

6-12. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP parts center in Mountain View, California.

b. No maximum or minimum on any mail order. There is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing.

c. Prepaid transportation. There is a small handling charge on each order.

d. No invoices - to provide these advantages, a check or money order must accompany each order.

6-13. Mail order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are located at the back of this manual.

6-14. EMULATOR POD DISASSEMBLY.

6-15. To gain access to the inside of the pod for parts replacement, perform the following steps. See figure 6-1a.

a. Lay the emulator pod on its top.

b. Remove the four round head screws near each rubber foot.

c. Remove the six flat head screws along each side of the pod.

d. Lift the bottom off the pod. The printed circuit boards are attached to the pod bottom.

e. Remove the two screws that secure the target cable assembly strain relief bracket; and remove the bracket from the pod bottom.

f. Loosen the emulator pod cable ground nut, and detach the emulator pod cable ground lug.

g. Remove the seven flat head screws that secure the two emulator boards to the pod bottom.

h. Slide the two boards out of the pod bottom.

6-16. TARGET PLUG DISASSEMBLY.

6-17. A 14 pin IC is the only replaceable part inside the target plug. To gain access to it, perform the following steps. See figure 6-1b.

a. There are two 40 pin sockets located in the plug housing. Carefully remove the first socket by gently prying at the ends. After the first socket is removed, carefully remove the second socket.

b. The replaceable IC is located in the center of the target plug printed circuit board. The IC is pressed into the printed circuit board; it is not soldered.

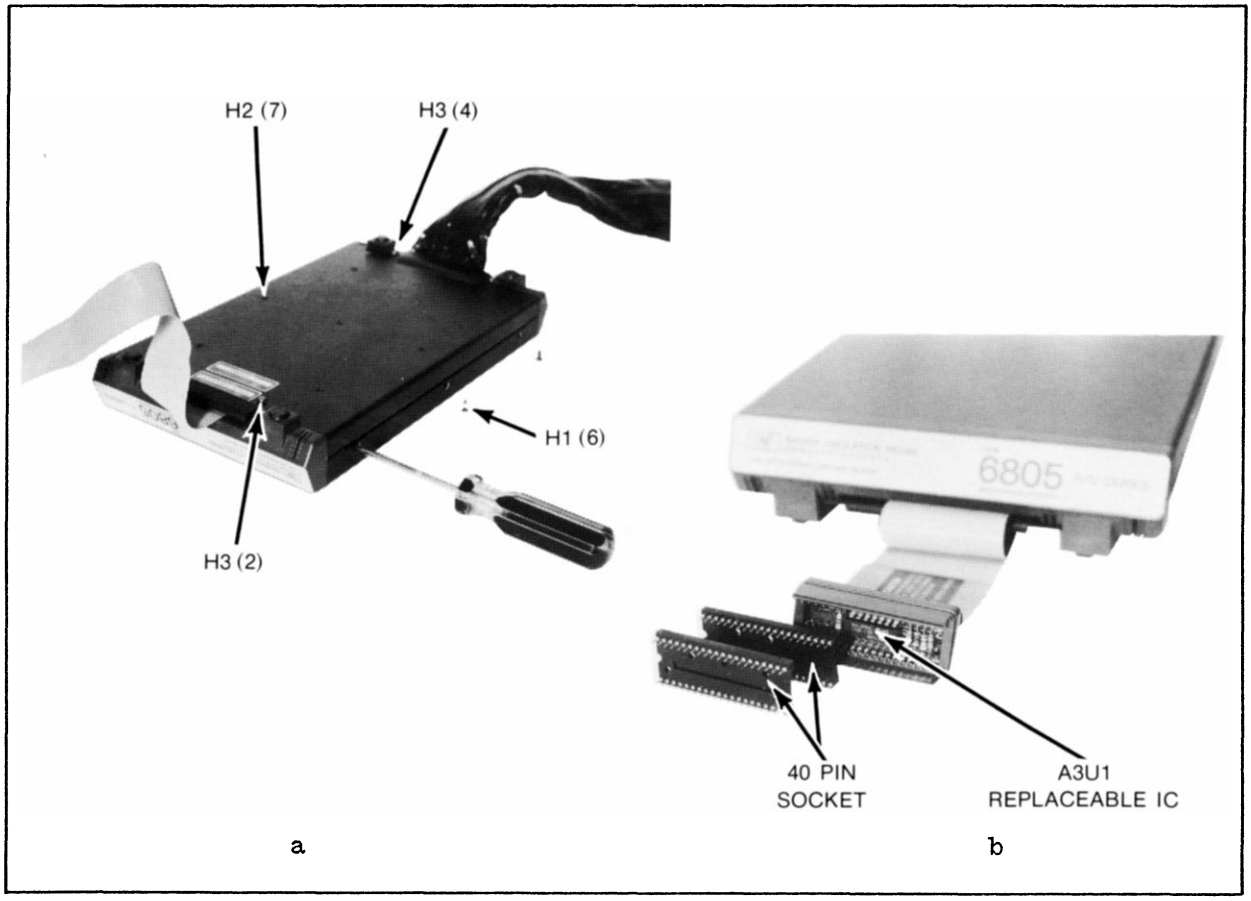


Figure 6-1. Disassembly

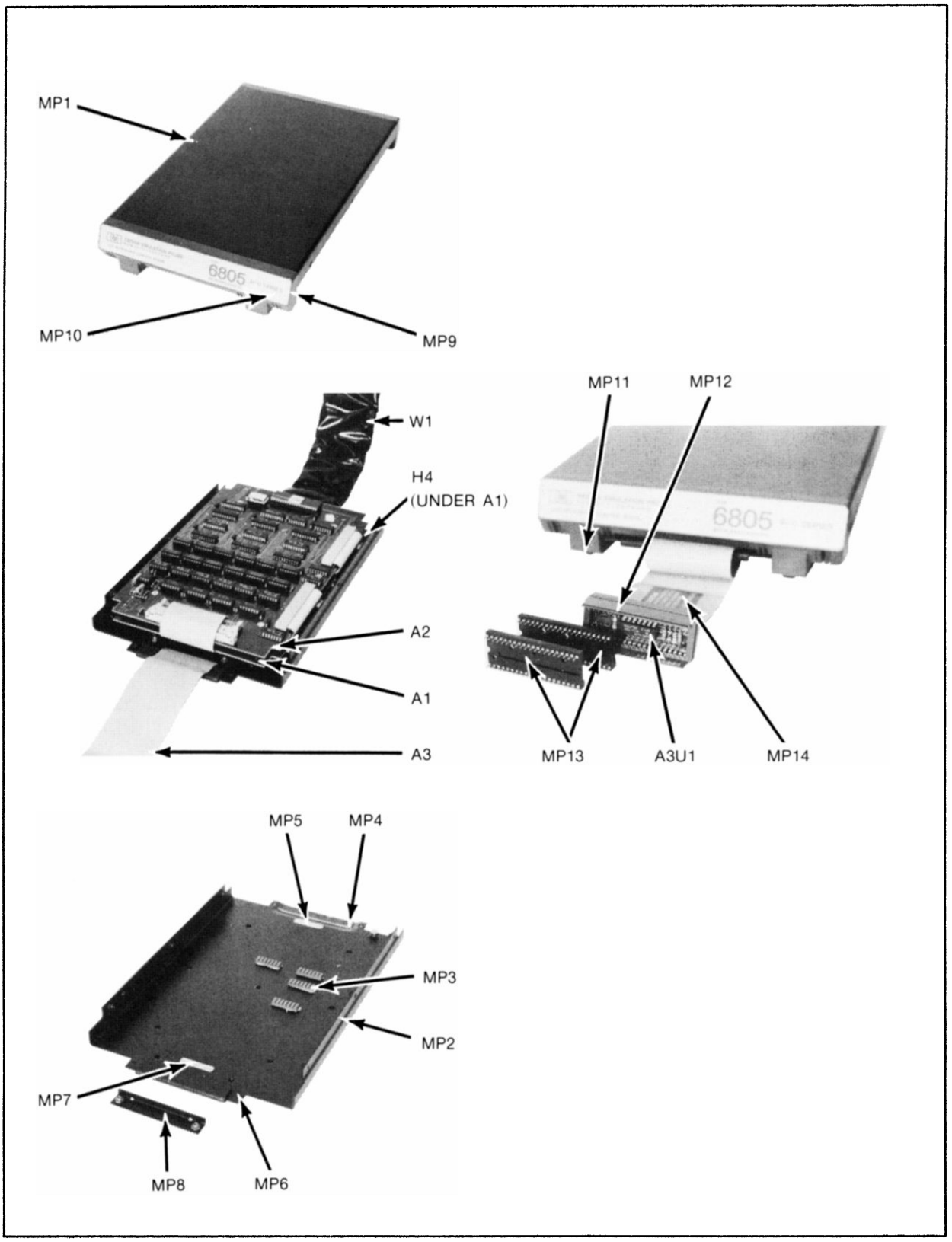


Figure 6-2. Mechanical Parts Locator

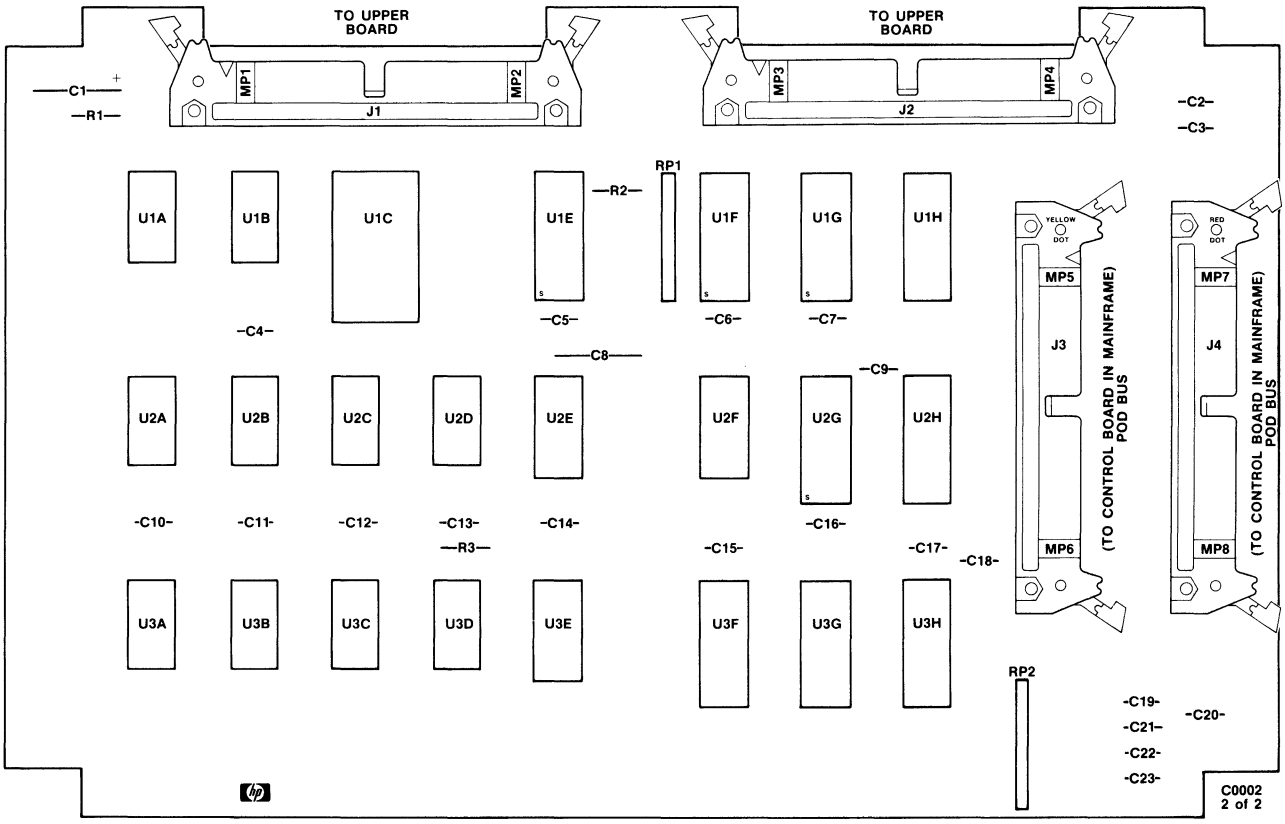


Figure 6-3. Lower Board Component Locator

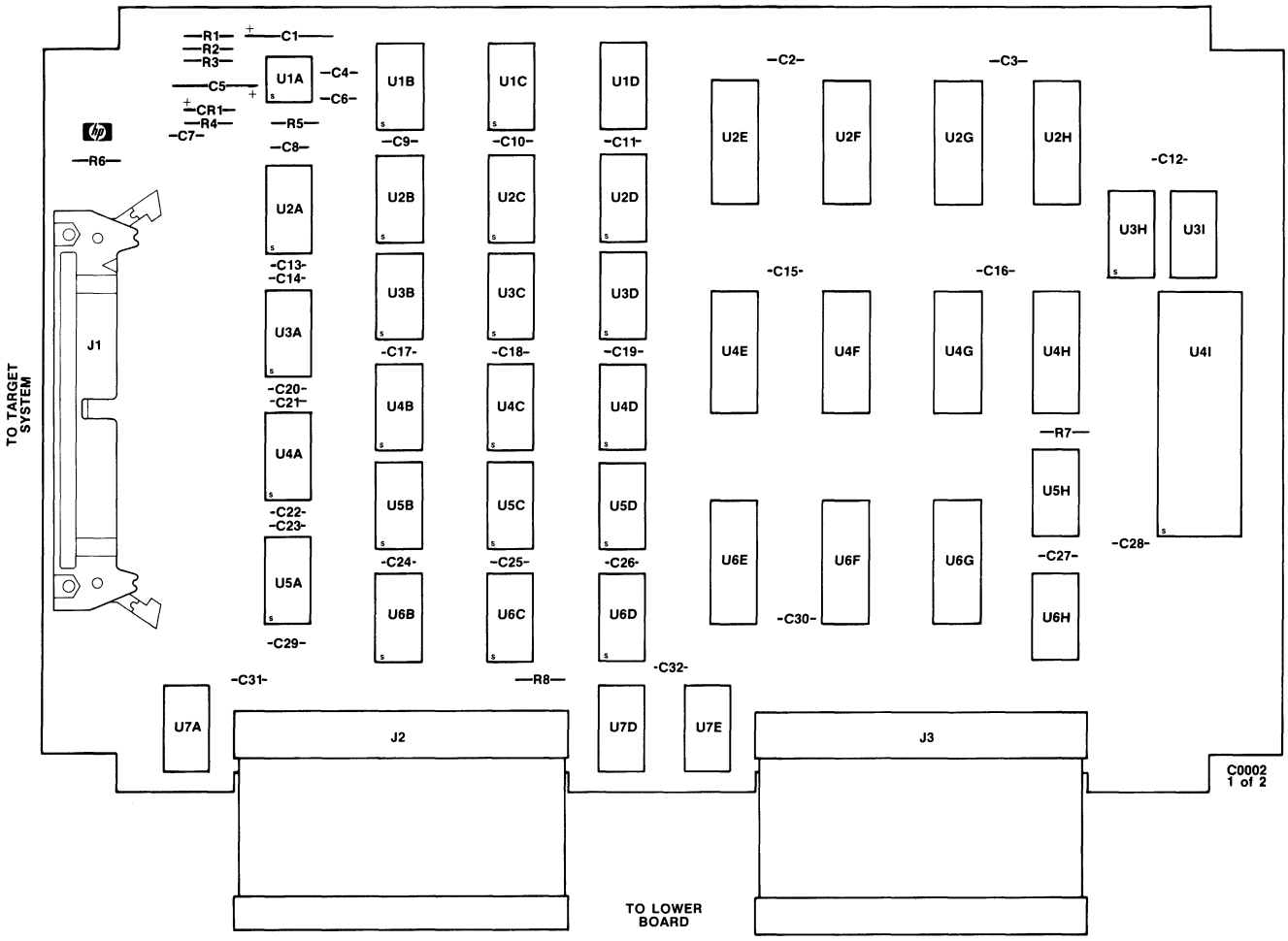


Figure 6-4. Upper Board Component Locator

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without

Table 6-2, Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	64192A	3	1	6805 R/U EMULATOR POD	28480	64192A
A1	64192-66501	5	1	ASSEMBLY-LOWER POD BOARD	28480	64192-66501
A1C1	0180-1746	5	2	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C2	0160-5321	8	51	CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A1C3	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A1C4	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A1C5	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A1C6	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A1C7	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A1C8	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C9	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A1C10	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A1C11	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A1C12	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A1C13	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A1C14	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A1C15	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A1C16	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A1C17	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A1C18	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A1C19	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A1C20	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A1C21	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A1C22	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A1C23	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A1J1	1251-5653	3	4	CONNECTOR- 50 PIN MREJT	28480	1251-5653
A1J2	1251-5653	3		CONNECTOR- 50 PIN MREJT	28480	1251-5653
A1J3	1251-5653	3		CONNECTOR- 50 PIN MREJT	28480	1251-5653
A1J4	1251-5653	3		CONNECTOR- 50 PIN MREJT	28480	1251-5653
A1MP1	1251-5595	2	8	POLARIZING KEY	28480	1251-5595
A1MP2	7124-0270	7		LABEL-YELLOW DOT	85480	QD25 TAPE B-810-YL
A1MP3	7124-0269	4		LABEL-RED DOT	85480	QD25 TAPE B-810-RD
A1R1	0757-0417	8	1	RESISTOR 562 1% .125W F TC=0+-100	24546	C4-1/8-T0-562R-F
A1R2	0757-0280	3	4	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R3	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1RP1	1810-0430	0	2	RESISTIVE NETWORK (SPECIAL)	28480	1810-0430
A1RP2	1810-0430	0		RESISTIVE NETWORK (SPECIAL)	28480	1810-0430
A1U1A	1820-1144	6	2	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A1U1B	1820-1197	9	3	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A1U1C	1820-0495	8	1	IC DCDR TTL 4-TO-16-LINE 4-INP	01295	SN74154N
A1U1E	1200-0639	8	4	SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1U1E	1820-1624	7	2	IC BFR TTL S OCTL 1-INP	01295	SN74S241N
A1U1F	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1U1F	1820-1676	9	2	IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
A1U1G	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1U1G	1820-1676	9		IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
A1U1H	1820-2024	3	6	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A1U2A	1820-1199	1	3	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A1U2B	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A1U2C	1820-1208	3	3	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A1U2D	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A1U2E	1820-1430	3	2	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A1U2F	1820-1217	4	1	IC MUXR/DATA-SEL TTL LS 8-TO-1-LINE	01295	SN74LS151N
A1U2G	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1U2G	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
A1U2H	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A1U3A	1820-1211	8	1	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A1U3B	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A1U3C	1820-1112	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A1U3E	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A1U3F	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A1U3G	1820-1997	7	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A1U3H	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A1U4D	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A1XU1A	1200-0638	7	24	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2	64192-66502	6	1	ASSEMBLY-UPPER POD BOARD	28480	64192-66502
A2C1	0180-1731	8	2	CAPACITOR-FXD 4.7UF+-10% 50VDC TA	56289	150D475X9050B2
A2C2	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C3	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C4	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C5	0180-1731	8		CAPACITOR-FXD 4.7UF+-10% 50VDC TA	56289	150D475X9050B2

See introduction to this section for ordering information

Table 6-2, Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2C6	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C7	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C8	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C9	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C10	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C11	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C12	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C13	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C14	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C15	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C16	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C17	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C18	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C19	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C20	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C21	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C22	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C23	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C24	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C25	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C26	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C27	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C28	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C29	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C30	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C31	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2C32	0160-5321	8		CAPACITOR-FXD CER 0.01UF 100VDC	28480	0160-5321
A2CR1	1901-0040	1	1	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A2J1	1251-6651	3	1	CONNECTOR	28480	1251-6651
A2J2	8120-3638	0	2	CABLE ASSEMBLY	28480	8120-3638
A2J3	8120-3638	0		CABLE ASSEMBLY	28480	8120-3638
A2R1	0757-0462	3	1	RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7502-F
A2R2	0757-0458	7	1	RESISTOR 51.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5112-F
A2R3	0757-0449	6	1	RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
A2R4	0757-0452	1	1	RESISTOR 27.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2742-F
A2R5	0757-0401	0	1	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A2R6	0757-0412	3	1	RESISTOR 365 1% .125W F TC=0+-100	24546	C4-1/8-T0-365R-F
A2R7	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R8	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2U1A	1820-0217	2	1	IC OP AMP GP 8-DIP-P PKG	28480	1820-0217
A2U1B	1820-1568	8	6	IC BFR TTL LS BUS QUAD	01295	SN74LS125AN
A2U1C	1820-1645	2	12	IC BFR TTL LS BUS QUAD	01295	SN74LS126AN
A2U1D	1820-1645	2		IC BFR TTL LS BUS QUAD	01295	SN74LS126AN
A2U2A	1906-0202	7	4	DIODE BRIDGE	01295	TID130
A2U2B	1820-1568	8		IC BFR TTL LS BUS QUAD	01295	SN74LS125AN
A2U2C	1820-1645	2		IC BFR TTL LS BUS QUAD	01295	SN74LS126AN
A2U2D	1820-1645	2		IC BFR TTL LS BUS QUAD	01295	SN74LS126AN
A2U2E	1820-1730	6	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A2U2F	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A2U2G	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A2U2H	1820-2102	8	2	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
A2U3A	1906-0202	7		DIODE BRIDGE	01295	TID130
A2U3B	1820-1568	8		IC BFR TTL LS BUS QUAD	01295	SN74LS125AN
A2U3C	1820-1645	2		IC BFR TTL LS BUS QUAD	01295	SN74LS126AN
A2U3D	1820-1645	2		IC BFR TTL LS BUS QUAD	01295	SN74LS126AN
A2U3H	1813-0174	5	1	OSCILLATOR- 4.00 MHZ	28480	1813-0174
A2U3I	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A2U4A	1906-0202	7		DIODE BRIDGE	01295	TID130
A2U4B	1820-1568	8		IC BFR TTL LS BUS QUAD	01295	SN74LS125AN
A2U4C	1820-1645	2		IC BFR TTL LS BUS QUAD	01295	SN74LS126AN
A2U4D	1820-1645	2		IC BFR TTL LS BUS QUAD	01295	SN74LS126AN
A2U4E	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A2U4F	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A2U4G	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A2U4H	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
A2U4I	1820-2930	0	1	MICROPROCESSOR MC6805R2	28480	1820-2930
A2U5A	1906-0202	7		DIODE BRIDGE	01295	TID130
A2U5B	1820-1568	8		IC BFR TTL LS BUS QUAD	01295	SN74LS125AN
A2U5C	1820-1645	2		IC BFR TTL LS BUS QUAD	01295	SN74LS126AN
A2U5D	1820-1645	2		IC BFR TTL LS BUS QUAD	01295	SN74LS126AN
A2U5H	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A2U6B	1820-1568	8		IC BFR TTL LS BUS QUAD	01295	SN74LS125AN
A2U6C	1820-1645	2		IC BFR TTL LS BUS QUAD	01295	SN74LS126AN
A2U6D	1820-1645	2		IC BFR TTL LS BUS QUAD	01295	SN74LS126AN
A2U6E	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A2U6F	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A2U6G	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A2U6H	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N

Table 6-2, Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A2U7A	1820-1207	2	2	IC GATE TTL LS NAND 8-INP	01295	SN74LS30N
A2U7D	1820-1207	2		IC GATE TTL LS NAND 8-INP	01295	SN74LS30N
A2U7E	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A2XU1A	1200-0796	8	1	SOCKET-IC 8-CONT DIP DIP-SLDR	28480	1200-0796
A2XU1B	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2XU1C	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2XU1D	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2XU2A	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2XU2B	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2XU2C	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2XU2D	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2XU3A	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2XU3B	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2XU3C	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2XU3D	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2XU3H	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2XU4A	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2XU4B	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2XU4C	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2XU4D	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2XU4I	1200-0654	7	1	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A2XU5A	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2XU5B	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2XU5C	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2XU5D	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2XU6B	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2XU6C	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A2XU6D	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A3	8120-3695	9	1	CABLE ASSEMBLY	28480	8120-3695
A3U1	1820-1198	0	1	IC-74LS03	01295	SN74LS03N
A4	64100-62102	4	1	ASSEMBLY-RFI GROUND BRACKET	28480	64100-62102
A4H1	2200-0512	7	6	SCREW-4-40 X .312	00000	ORDER BY DESCRIPTION
A4H1	2360-0129	0	1	SCREW-MACH 6-32 1-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A4H2	2200-0510	5	7	SCREW- 4-40 X .750	00000	ORDER BY DESCRIPTION
A4H2	2420-0001	5	2	NUT-HEX-W/LKWR 6-32-THD .109-IN-THK	00000	ORDER BY DESCRIPTION
A4H3	2200-0105	4	10	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A4H4	2200-0151	0	2	SCREW-MACH 4-40 .75-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A4H4	2420-0001	5		NUT-HEX-W/LKWR 6-32-THD .109-IN-THK	00000	ORDER BY DESCRIPTION
A4H5	3050-0235	3	2	WASHER-FL MTLC NO. 4 .117-IN-ID	28480	3050-0235
A4H6	2360-0117	6	2	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A4MP1	64100-01205	0	1	RFI GROUND BRACKET	28480	64100-01205
A4MP2	1531-0273	7	1	CLAMP-BAR	28480	1531-0273
A4MP3	4040-1907	8	4	HEAT SINK-RUBBER	28480	4040-1907
A4MP4	0400-0251	3		RUBBER-TRIM	28480	0400-0251
A4MP6	5001-0440	1		TRIM-SIDE	28480	5001-0440
A4MP9	5041-1575	9	2	PROBE-END CAP	28480	5041-1575
A4MP10	7121-3021	6	2	LABEL-EMULATION	28480	7121-3021
A4MP11	0403-0179	0	4	BUMPER-PLASTIC	28480	0403-0179
A4MP12	4040-1573	4	1	HOOD-PIN GUARD	28480	4040-1573
A4MP13	1200-0682	1	2	SOCKET-40 PIN AG	28480	1200-0682
A4MP14	7121-3182	0	1	LABEL-CABLE "CAUTION"	28480	7121-3182
	64192-62101	3	1	POD ASSEMBLY	28480	64192-62101
MP1	64256-04102	9	1	TOP COVER	28480	64256-04102
MP2	64192-04101	1	1	BOTTOM COVER	28480	64192-04101
MP5	64222-94303	1	1	LABEL-LONG CABLE	28480	64222-94303
MP7	64222-94304	2	1	LABEL-SHORT CABLE	28480	64222-94304
MP8	64192-04102	2	1	STRAIN RELIEF BRACKET	28480	64192-04102
W1	64192-61602	7	1	EMULATOR POD CABLE	28480	64192-61602

See introduction to this section for ordering information

Table 6-3. List of Manufacturers' Codes

Mfr No.	Manufacturers Name	Address		Zip Code
00000	ANY SATISFACTORY SUPPLIER			
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
85480	BRADY W H CO	MILWAUKEE	WI	53209

SECTION VII

MANUAL CHANGES

This section normally contains backdating information for models with repair numbers prior to the one shown on the title page. Because this edition includes only the first repair number, there is no backdating material.

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2. This section contains reference information for servicing the Model 64192A 6805 R/U Emulator Pod. For convenience, the schematics, component locator, and other service information are provided on foldout sheets.

8-3. The purpose of the emulator pod is to act as the user microcomputer while simultaneously making internal microcomputer signals accessable to the emulation subsystem. To do this, two printed circuit boards duplicate the 6805 R/U internal address and data bus, bidirectional ports, port data register, port data-direction registers, timer, and timer prescaler. The following functional blocks implement these operations.

Upper Board, Assembly A2	Schematic
MC6805R2 Microcomputer	1
Crystal Select Logic	1
User-Crystal Interface	2
Internal Register Control	1
Data-out Latch	1
Port Input buffer & Data-In Latch	1
Port Buffers and Control	1, 2

Lower Board, Assembly A1	
Internal Register Monitor	3
Prescaler Logic	4
Timer Logic	3, 4
Pod Option Buffer	3
Data Buffers	3
Address Latches	3

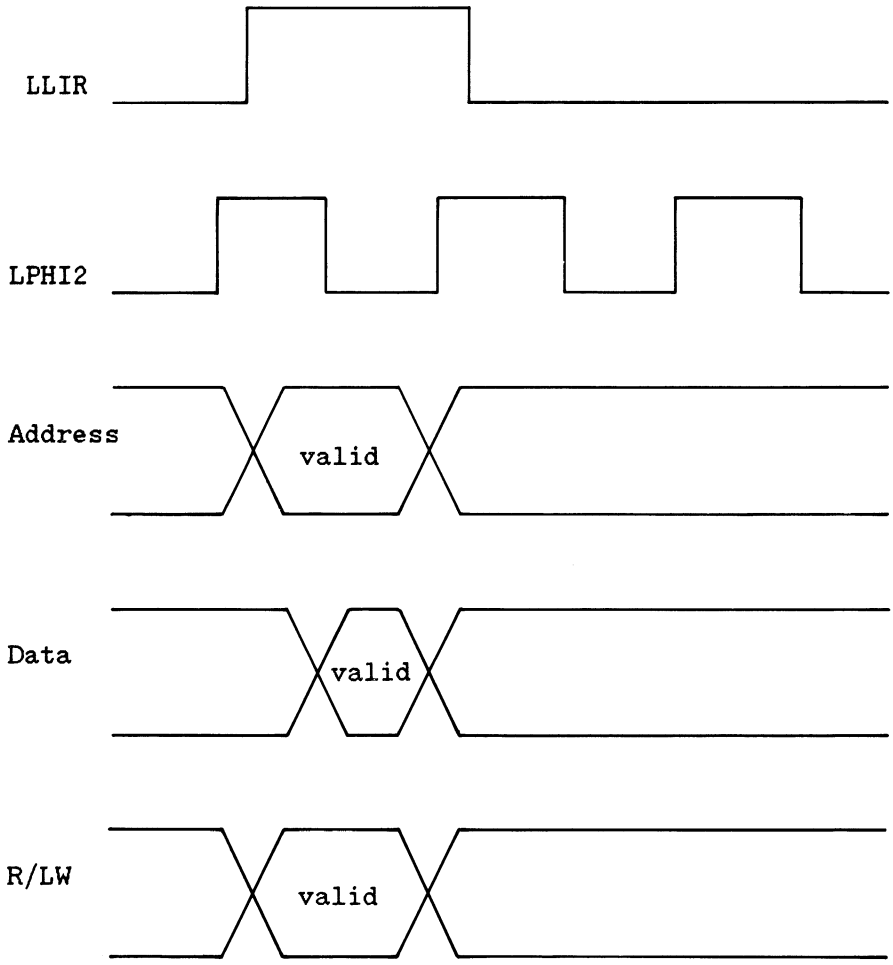
8-4. CIRCUITRY DESCRIPTIONS. Refer to block diagram, figure 8-4 and to the fold out schematics.

8-5. CRYSTAL SELECT LOGIC, SCHEMATIC 1.

8-6. The 6805R2 emulator processor can be clocked by one of two sources; a 4MHz crystal located on the upper board, or a user clock located in the target system. During emulation, the user can enter the choice of clock through the development station display. Signal LEXT is generated on the emulator controller and passed to the upper pod board where gates U3I select either the user supplied clock, or the 4MHz clock from crystal U3H.

8-7. MC6805R2 MICROCOMPUTER, SCHEMATIC 1.

8-8. Chip U4I is the emulator processor. It is an MC6805R2 with its timer prescaler factory masked as divide-by-one. A timing diagram is shown below.



8-9. Signal LLIR is the load instruction register bit from the processor. It goes low when the processor fetches the first byte of an opcode. LPHI2 is one of the clock signals produced by the on-chip clock circuit of the processor. The processor produces R/LW to indicate when a read or write operation is to occur. The default status of this signal is read, and when the processor is halted, the status remains in the read state.

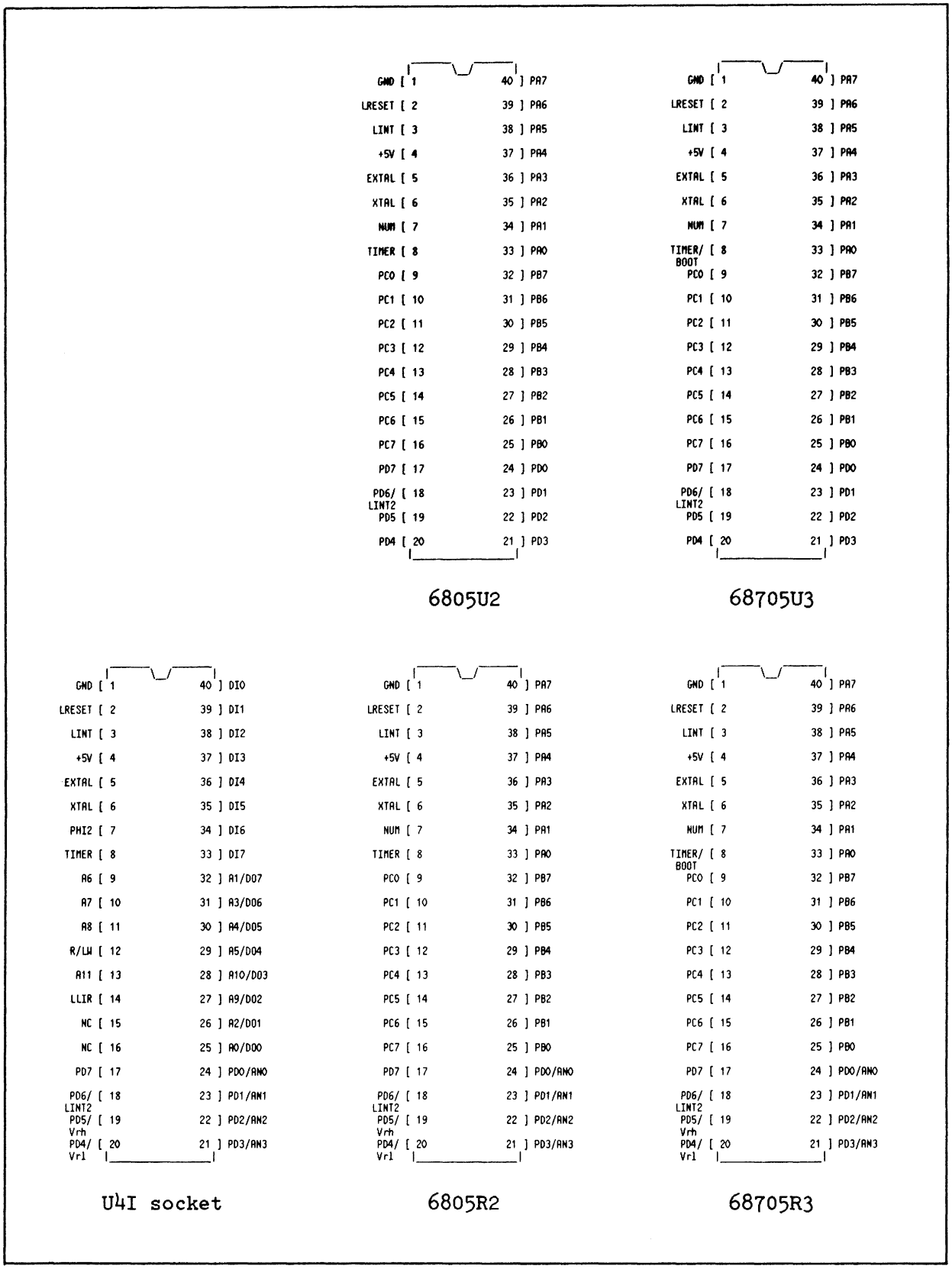


Figure 8-1. 6805 R/U Microcomputer Pinouts

8-10. USER-CRYSTAL INTERFACE, SCHEMATIC 2.

8-11. Op-amp U1A provides the bias for the oscillator in the target plug. Several discrete componets make up the waveforming and timing circuit to supply the emulator processor with a TTL-level clock signal. This circuit works in conjunction with active components in the target plug to compensate for the long cable length between the user system clock source and the processor in the pod.

8-12. INTERNAL REGISTER CONTROL, SCHEMATIC 1.

8-13. The first sixteen addresses of the emulator processor are internal registers. Some of these registers have been reproduced in discrete components on the upper pod board, while some remain internal to the processor. The internal register control is used to control reads and writes to these sixteen registers so that the appropriate discrete components or internal registers are selected. The emulator processor reads an internal register, and places the data on the data-out bus.

8-14. Signals LSEL0-15 indicate which internal address is being selected. Gates U6H and U7E pass six of these signals to clock the port A, B, and C data-direction registers and data output registers.

8-15. Gates U7A, U7D, and U7E form a multiple input OR gate that detects which internal register is being accessed. The gate produces the read internal (RINT) signal which gates data-out bits back into the processor via the datain bus. The timer control register U3G is selected by LSEL9, using circuitry on the pod lower board.

8-16. DATA-OUT LATCH, SCHEMATIC 1.

8-17. To catch and hold the data coming out of the emulator processor, latch U2H is used. This latch is clocked by the internal processor clock LPHI2.

8-18. PORT INPUT BUFFERS AND DATA-IN LATCH, SCHEMATIC 1.

8-19. Inputs on bidirectional ports A, B, and C are buffered from the target system by chips U2G, U4G, and U6G respectively. These inputs are passed through the buffers and latched as data-in bits on U4H for direct input into the emulator processor.

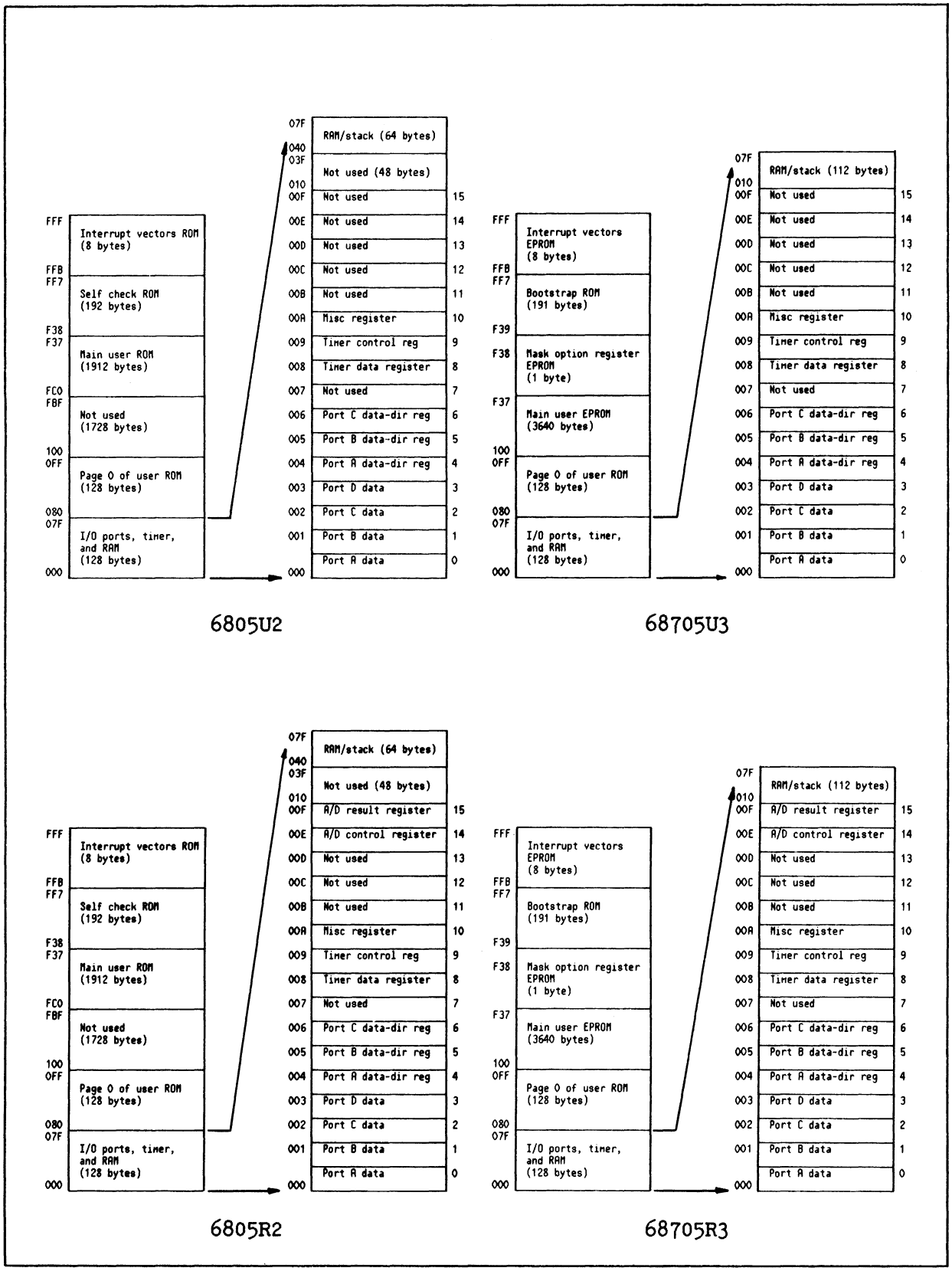


Figure 8-2. 6805 R/U Memory Address Maps

8-20. PORT BUFFERS AND CONTROL, SCHEMATICS 1, 2.

8-21. On schematic 2 are located all of the bidirectional port buffers. Each bidirectional port that is normally internal to the emulator processor is implemented in six external components. For example, in port A, chips U2D, U2C, U1D, and U1C, buffer output data. Chips U2B, and U1B, buffer input data. All port lines have diodes connected to ground to eliminate electrostatic voltage spikes.

8-22. Port control is accomplished by six chips shown on schematic 1. Three of the chips; U2E, U4E, and U6E, provide internal data-direction registers for ports A, B, and C. Each register contains eight bits to set each port bit as input or output. This hardware is necessary because the user can, via software, set each port bit to be input or output.

8-23. Also, three eight bit latches, U2F, U4f, and U6F are part of the port control function. These latches, which are normally internal to the emulator processor, are used to hold port data that is being output from the emulator processor.

8-24. INTERNAL REGISTER MONITOR, SCHEMATIC 3.

8-25. When LPORTS is low, the four least significant bits on the address bus represent the sixteen internal register addresses of the emulator processor. Data decoder U1C monitors these low bits, detects which internal register address is being accessed, and produces a low signal on the appropriate LSEL line. The LSEL0-15 lines are then used to control read or write at the selected register. See internal register control, schematic 1.

8-26. PRESCALER LOGIC, SCHEMATIC 4.

8-27. During emulation, the user can enter the choice of timer prescaler factor through the mainframe display. This choice allows simulation of seven prescaler hardware mask options.

8-28. The internal timer prescaler of the emulator processor is reproduced in discrete components on the lower pod board. Chips U3E and U2E are connected together to produce seven output frequencies that are proportional to the input clock. Being binary counters, the output frequencies represent the input clock frequency divided by 2, 4, 8, 16, 32, 64, and 128.

8-29. Data selector U2F acts as the timer prescaler by enabling only one of the seven frequencies from the counter to pass. Timing control register bits TCR0-2 are decoded to select the appropriate prescaling factor. When TCR0-2 are all low, the frequency selected at pin 4 comes from flip-flop U3D, pin 5, which is the prescaler by-pass. This frequency is equivalent to a prescaler factor of 1.

8-30. The output from U2F passes through flip-flops U3C, U3D, and exculsive OR gate U3A. These components shape the timing waveform and sychronize it with the emulator processor clock signal LMEM.

8-31. TIMER LOGIC, SCHEMATICS 3, 4.

8-32. During emulation, the user can enter through the mainframe display a choice of timer clock source, either internal or external, and also whether the timer clock is turned off, on, or is software-gated. The circuitry that implements these choices consists of several gates on the lower pod board. Gates in U2D receive the HTIMER and TCR5 signals to choose between the internal LPHI2 signal or the user's external clock. Gates in U1B and U3A select whether the timer clock is off, on, or gated under software control.

8-33. Chip U3G reproduces the on-chip timer control register. This eight bit latch holds timer control bits that set the timer prescaler, prescaler clear, software-gating of the timer, internal/external timer, timer interrupt mask, and timer interrupt request.

8-34. POD OPTION BUFFER, SCHEMATIC 3.

8-35. Buffer U3F isolates pod option signals from the emulator controller and the pod itself. These signals set up the user specified 6805 emulator configuration.

8-36. DATA BUFFERS, SCHEMATIC 3.

8-37. Four buffers are used to control signal flow on the various data buses. Chip U1H is a buffer between the data-out bus and the data-in bus. It is clocked by the Read Internal (RINT) signal and places data coming from emulator processor immediately back onto the data-in bus so that internal registers can be read.

8-38. Data coming from the emulator processor is buffered from the data-out bus by U2G, while data coming into the emulator processor is buffered by U2H. Timer Control bits are buffered from the emulator processor by U3H.

8-39. ADDRESS LATCHES, SCHEMATIC 3.

8-40. Address bits from the emulator processor are latched into chips U1G and U1F. Because of the limited addressing range of 6805 family processors, only twelve bits of address are placed on the sixteen bit emulator pod address bus.

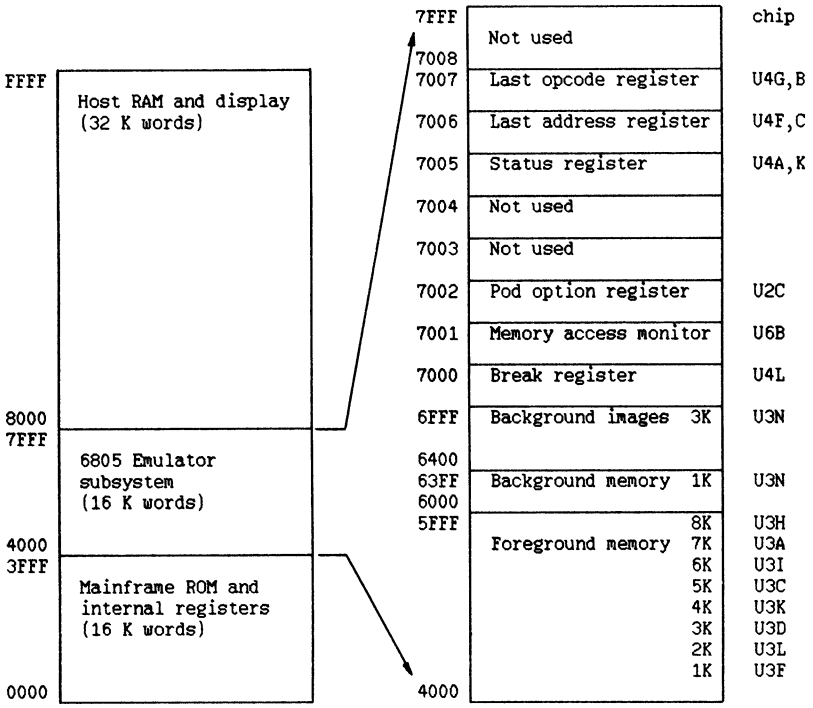


Figure 8-3. Emulator Subsystem Memory Map

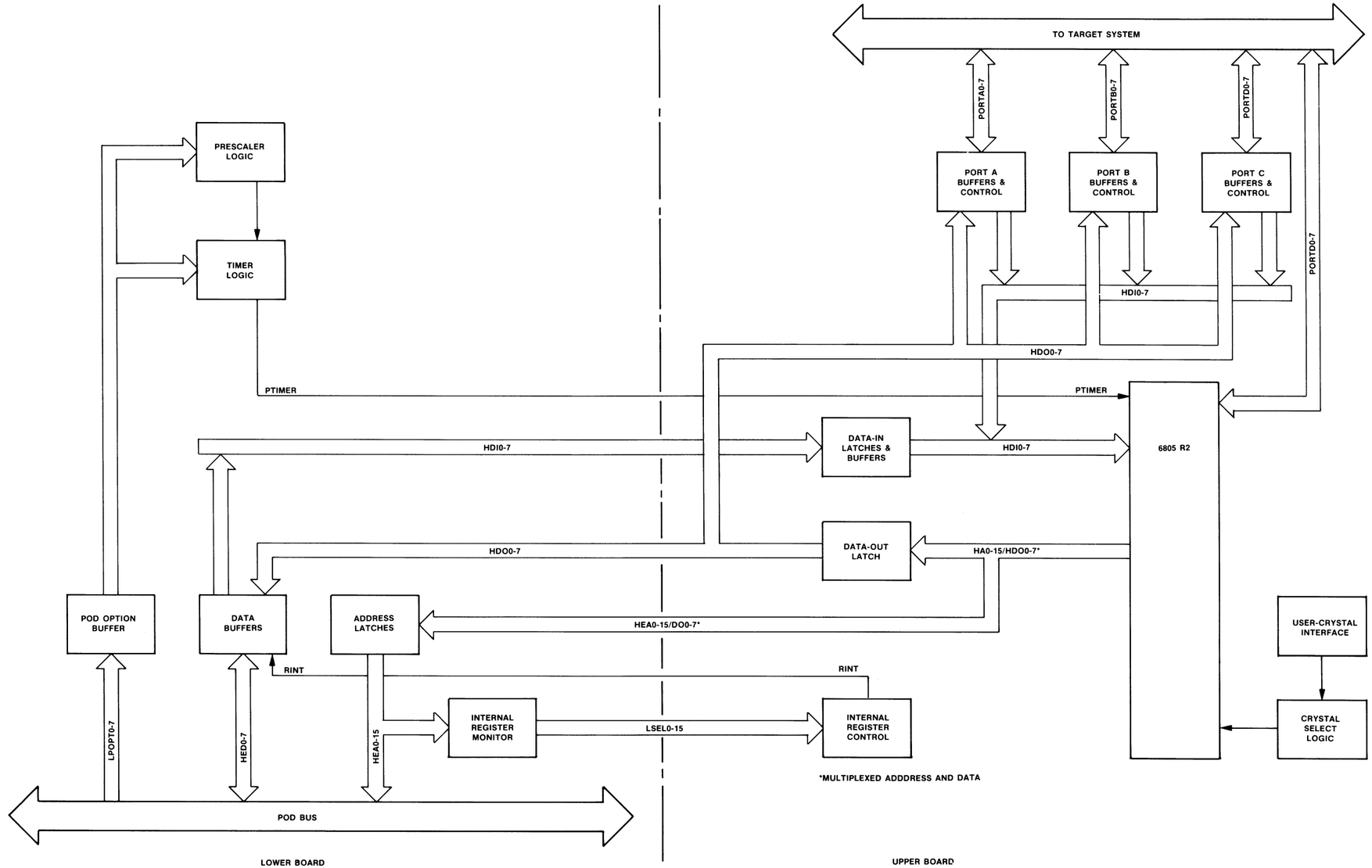


Figure 8-4. Emulator Pod Block Diagram

Table 8-1. Connector Signals

Lower Board, Assembly A1.

Connector A1 J1		Connector A1 J2		Connector A1 J3		Connector A1 J4	
Schematic 4		Schematic 3		Schematic 3		Schematic 4	
Pin		Pin		Pin		Pin	
1	LSEL15	1	LPHI2	1	HEA15	1	LMEM
2	gnd	2	gnd	2	gnd	2	gnd
3	LSEL14	3	HA12	3	HEA14	3	LREAD
4	LSEL13	4	HA11	4	gnd	4	gnd
5	gnd	5	gnd	5	HEA13	5	HOPFETCH
6	LSEL12	6	HA10/DO3	6	gnd	6	gnd
7	LSEL11	7	HA9/DO2	7	HEA12	7	LEXT
8	gnd	8	gnd	8	gnd	8	+ 5 v
9	LSEL10	9	HA8	9	HEA11	9	BLRESET
10	LSEL9	10	HA7	10	gnd	10	gnd
11	gnd	11	gnd	11	HEA10	11	LFG
12	LSEL8	12	HA6	12	gnd	12	+ 5 v
13	LSEL7	13	HA5/DO4	13	HEA9	13	LPORTS
14	gnd	14	gnd	14	gnd	14	gnd
15	LSEL6	15	HA4/DO5	15	HEA8	15	HUSER
16	LSEL5	16	HA3/DO6	16	gnd	16	+5 v
17	gnd	17	gnd	17	HEA7	17	HFGMEM
18	LSEL4	18	HA2/DO1	18	gnd	18	gnd
19	LSEL3	19	HA1/DO7	19	HEA6	19	HDEFIB
20	+5 v	20	+5 v	20	gnd	20	+5 v
21	LSEL2	21	HA0/DO0	21	HEA5	21	LIRQ
22	LSEL1	22	HD7	22	gnd	22	gnd
23	gnd	23	gnd	23	HEA4	23	HTIMER
24	LSEL0	24	HD6	24	gnd	24	+5 v
25	RINT	25	HD5	25	HEA3	25	LPSTAT3
26	+5 v	26	+5 v	26	gnd	26	gnd
27	LEXT	27	HD4	27	HEA2	27	LPSTAT4
28	gnd	28	HD3	28	gnd	28	+5 v
29	LRESET	29	gnd	29	HEA1	29	LPSTAT5
30	gnd	30	HD2	30	gnd	30	gnd
31	LIRQ	31	HD1	31	HEA0	31	LPSTAT6
32	+5 v	32	+5 v	32	gnd	32	gnd
33	HTIMER	33	HD0	33	HED7	33	LICE
34	gnd	34	HDI7	34	gnd	34	gnd
35	LPSTAT3	35	gnd	35	HED6	35	LPOPT0
36	gnd	36	HDI6	36	gnd	36	gnd
37	LPSTAT4	37	HDI5	37	HED5	37	LPOPT1
38	gnd	38	gnd	38	gnd	38	gnd
39	LPSTAT5	39	HDI4	39	HED4	39	LPOPT2
40	gnd	40	HDI3	40	gnd	40	PID0
41	LPSTAT6	41	gnd	41	HED3	41	LPOPT3
42	POWER	42	HDI2	42	gnd	42	PID1
43	LICE	43	HDI1	43	HED2	43	LPOPT4
44	PID0	44	gnd	44	gnd	44	PID2
45	PTIMER	45	HDI0	45	HED1	45	LPOPT5
46	PID1	46	AS	46	gnd	46	PID3
47	PIRQ	47	+12 v	47	HED0	47	LPOPT6
48	PID2	48	LI	48	gnd	48	+12 v
49	BLRESET	49	- 5.2 v	49	not used	49	LPOPT7
50	PID3	50	LR/W	50	-5.2 v	50	+12 v
To A2 J2		To A2 J3		To 64191A J1		To 64191A J4	

Upper Board, Assembly A2.

Connector A2 J1		Connector A2 J2		Connector A2 J3	
Schematic 2		Schematic 1		Schematic 1	
Pin		Pin		Pin	
1	gnd	1	LSEL15	1	LPHI2
2	gnd	2	gnd	2	gnd
3	gnd	3	LSEL14	3	HA12
4	gnd	4	LSEL13	4	HA11
5	gnd	5	gnd	5	gnd
6	PORTA7	6	LSEL12	6	HA10/DO3
7	LRESET	7	LSEL11	7	HA9/DO2
8	PORTA6	8	gnd	8	gnd
9	LIRQ	9	LSEL10	9	HA8
10	PORTA5	10	LSEL9	10	HA7
11	POWER	11	gnd	11	gnd
12	PORTA4	12	LSEL8	12	HA6
13	USEREXTAL	13	LSEL7	13	HA5/DO4
14	PORTA3	14	gnd	14	gnd
15	USERXTAL	15	LSEL6	15	HA4/DO5
16	PORTA2	16	LSEL5	16	HA3/DO6
17	LPSTAT6	17	gnd	17	gnd
18	PORTA1	18	LSEL4	18	HA2/DO1
19	HTIMER	19	LSEL3	19	HA1/DO7
20	PORTA0	20	+5 v	20	+5 v
21	PORTC0	21	LSEL2	21	HA0/DO0
22	PORTB7	22	LSEL1	22	HD7
23	PORTC1	23	gnd	23	gnd
24	PORTB6	24	LSEL0	24	HD6
25	PORTC2	25	RINT	25	HD5
26	PORTB5	26	+5 v	26	+5 v
27	PORTC3	27	LEXT	27	HD4
28	PORTB4	28	gnd	28	HD3
29	PORTC4	29	LRESET	29	gnd
30	PORTB3	30	gnd	30	HD2
31	PORTC5	31	LIRQ	31	HD1
32	PORTB2	32	+5 v	32	+5 v
33	PORTC6	33	HTIMER	33	HD0
34	PORTB1	34	gnd	34	HDI7
35	PORTC7	35	LPSTAT3	35	gnd
36	PORTB0	36	gnd	36	HDI6
37	PORTD7	37	LPSTAT4	37	HDI5
38	PORTD0	38	gnd	38	gnd
39	PORTD6	39	LPSTAT5	39	HDI4
40	PORTD1	40	gnd	40	HDI3
41	PORTD5	41	LPSTAT6	41	gnd
42	PORTD2	42	POWER	42	HDI2
43	PORTD4	43	LICE	43	HDI1
44	PORTD3	44	PID0	44	gnd
45	gnd	45	PTIMER	45	HDI0
46	gnd	46	PID1	46	AS
47	gnd	47	PIRQ	47	+12 v
48	gnd	48	PID2	48	LI
49	gnd	49	BLRESET	49	- 5.2 v
50	gnd	50	PID3	50	LR/W
To Target		To A1 J1		To A1 J2	

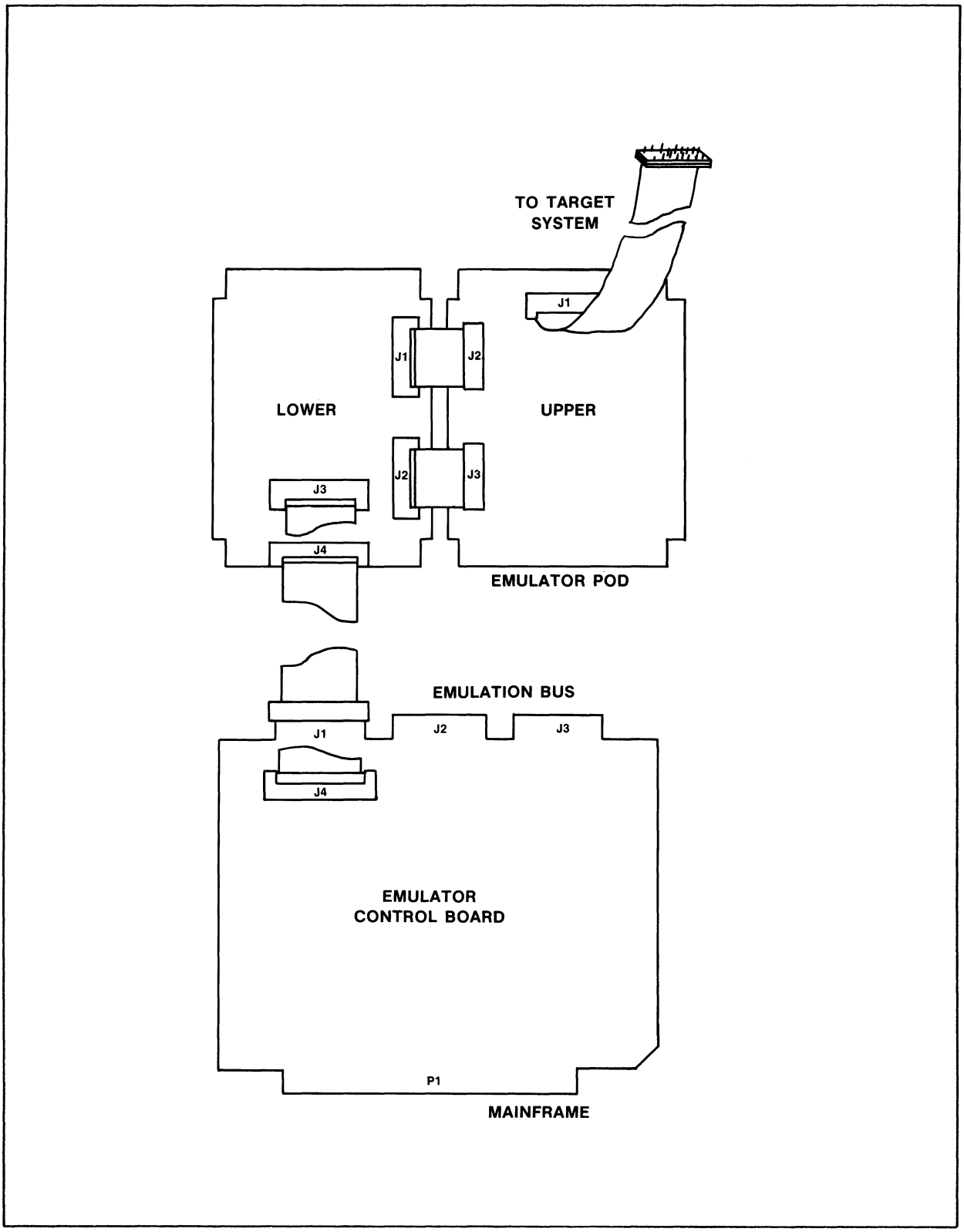


Figure 8-5. Connector Diagram

Table 8-2. Mnemonics

Mnemonic	Description
ADDR0-7	Port A Data Direction Register Bus 0-7. Eight bits that control emulator processor port A data direction, ie., input or output. Schematics 1*, 2.
AS	Address Strobe. When high, the multiplexed HA0-12/DO0-7 address/data bus has an address on it. When low, there is data on the bus. Schematics 1*, 3.
BDDR0-7	Port B Data Direction Register Bus 0-7. Eight bits that control emulator processor port B data direction, ie., input or output. Schematics 1*, 2.
BLRESET	Buffered Low Reset. Derived from LRESET, it resets the emulator processor. Schematics 1, 4*.
CDDR0-7	Port C Data Direction Register Bus 0-7. Eight bits that control emulator processor port C data direction, ie., input or output. Schematics 1*, 2.
DO0-7	Data-Out Bus 0-7. External version of emulator processor on-chip data bus. It is unidirectional output from the processor, multiplexed with eight bits of address in the HA0-12 bus. Schematics 1*, 3.
HA0-12	High Address Bus 0-12. External version of the emulator processor on-chip address bus. Eight of the bits are multiplexed with the DO0-7 data bus. Schematics 1*, 3.
HD0-7	High Data Bus 0-7. Latched, or demultiplexed, version of DO0-7. It is unidirectional output from the emulator processor. Schematics 1*, 3.

* indicates signal source.

Table 8-2. Mnemonics (Cont'd)

Mnemonic	Description
HDEFIB	High Defibrillate. Inverted LDEFIB; initializes the emulator pod to a known state. Also, it produces BLRESET. Schematic 4.
HDI0-7	High Data Input Bus 0-7. Data input to the emulator processor. It is derived from ports A, B, C data; by reading the DO0-7 data bus; or from the HED0-7 data bus. Schematics 1*, 3*.
HED0-7	High Emulator Data Bus 0-7. Bidirectional data bus between the emulator pod and the emulator controller. Schematic 3.
HED3	High Emulator Data Line 3. Sets timing control register bit. Schematics 3*, 4.
HOPFETCH	High Opcode Fetch. Indicates the emulator processor is fetching an opcode from memory. It is derived from signal LI and passed to the controller. Schematic 4.
HTIMER	High Timer. Signal directly from user target system plug. Enables timer circuitry on the pod to count. It is used on the controller to indicate timer status. Schematics 1, 2*.
HUSER	High User. Signal from the controller; indicates an emulator processor access to memory below address 64. Schematics 3, 4*.
LEXT	Low External. Signal from development station; when low, selects external clock source on the user target system. When high, selects 4 MHz crysta located on the pod. Schematics 1, 4*.

* indicates signal source.

Table 8-2. Mnemonics (Cont'd)

Mnemonic	Description
LFG	Low Foreground. Indicates the emulator is executing in foreground memory. Schematic 4.
LI	Load Instruction. When high, indicates the emulator processor is loading an opcode into its instruction register. Produces HOPFETCH. Schematics 1*, 3, 4.
LICE	Low In-ciruit Emulation. Indicates target system plug is receiving +5v from user hardware. It is derived from POWER signal. Schematics 1 (no connection), 4*.
LIRQ	Low Interrupt Request. Signal directly from the target system plug; indicates the target hardware has issued an interrupt request. Schematics 1, 2*.
LMEM	Low Memory. Clock from emulator processor. When low, address lines contain address. When high, data lines contain valid data. It is functionally the same signal as LPHI2. Schematics 3*, 4.
LPHI2	Low Phi 2. Clock from emulator processor. When low, the address bus has an address on it. When high, the data bus has data on it. Schematics 1*, 3, 4.
LPOPT0-7	Low Pod Option Bus 0-7. Option control bits from the development station. These bits implement the microcomputer emulation choices entered by the development station user. Uses negative logic; high = 0, low = 1. Schematics 3, 4*.

* indicates signal source.

Table 8-2. Mnemonics (Cont'd)

Mnemonic	Description
LPORTS	Low Ports. Indicates the emulator processor is accessing memory in the range 0-15. These addresses are primarily for ports/timer. Schematics 3, 4*.
LPSTAT0-7	Low Pod Status Bus 0-7. Bits that indicate status of pod. The following bits have specific assigned names: 0 = LRESET, 1 = LIRQ, 2 = HTIMER, 6 = target plug, pin 7, 7 = LICE. Uses negative logic; high = 0, low = 1. Schematics 1*, 4*.
LPSTAT3-5	Low Pod Status Bus 3-5. Three status bits of LPSTAT0-7 bus. Uses negative logic; high = 0, low = 1. Schematics 1*, 4*.
LR/W	Low Read/High Write. Signal from the emulator processor that indicates it is ready to read data. It produces LREAD. Schematics 1*, 3, 4.
LREAD	Low Read. Derived from LR/W, it indicates the emulator processor is ready to read data. This signal is sent to the controller. Schematic 4*.
LRESET	Low Reset. Signal directly from target system plug; indicates the target hardware has requested a reset. It also produces BLRESET. Schematics 1, 2*, 4.
LSEL0-15	Low Select Bus 0-15. These bits are produced by the internal register monitor. They indicate an address in the range 0-15 is being accessed. Schematics 1, 3*, 4.

* indicates signal source.

Table 8-2. Mnemonics (Cont'd)

Mnemonic	Description
PAD0-7	Port A Data Bus 0-7. Unidirectional data lines from the emulator processor to the port A data buffers. Schematics 1*, 2.
PBD0-7	Port B Data Bus 0-7. Unidirectional data lines from the emulator processor to the port B data buffers. Schematics 1*, 2.
PCD0-7	Port C Data Bus 0-7. Unidirectional data lines from the emulator processor to the port C data buffers. Schematics 1*, 2.
PCTL1-6	Port Control Bus 1-6. On rising edge, clocks ports A, B, and C data latches and data direction latches. Schematic 1.
PID0-3	Pod Identification Bus 0-3. Four bits that uniquely identify the attached emulator pod. Originates on the pod and is passed by the controller to the development station on the LD0-15 data bus. Schematics 1*, 4.
PIRQ	Pod Interrupt Request. Signal derived from LIRQ that interrupts the emulator processor. Schematics 1, 4*.
PORTA0-7	Port A Data Bus 0-7. Bidirectional data bus between the pod and the target system. Schematics 1, 2*.
PORTB0-7	Port B Data Bus 0-7. Bidirectional data bus between the pod and the target system. Schematics 1, 2*.

* indicates signal source.

Table 8-2. Mnemonics (Cont'd)

Mnemonic	Description
PORTC0-7	Port C Data Bus 0-7. Bidirectional data bus between the pod and the target system. Schematics 1, 2*.
PORTD0-7	Port D Data Bus 0-7. Unidirectional data bus from the target system to the pod. Schematics 1, 2*.
POWER	Power. Signal directly from the target system plug; indicates the plug is receiving +5v from the target system. It produces the LICE signal. Schematics 1, 2*, 3.
PTIMER	Pod Timer. Signal produced by timer control circuitry on the pod that controls the emulator processor on-chip timer. Schematics 1, 4*.
RINT	Read Internal. Signal derived from LSEL0-15 that enables the emulator processor to read its own internal registers and place the data on the DO0-7 data-out bus. Schematics 1*, 3, 4.
TCR0-5	Timer Control Register Bits 0-5. External versions of the on-chip timer control register; the function varies with microcomputer being emulated. In general, the function are: bits 0,1,2 = prescaler select, 3 = prescaler clear (see HED3), 4 = timer external input enable, 5 = timer input select. Schematics 3*, 4.
TCRCLK	Timer Control Register Clock Bit. External version of the on-chip timer control register select line. Allows access to address 9, the timer control register. Schematics 3*, 4.

* indicates signal source.

Table 8-2. Mnemonics (Cont'd)

Mnemonic	Description
USEREXTAL	User External Crystal. Signal directly from the target system plug that can be used as the emulator processor clock source. The clock is produced by a physically separate crystal in the target system. Schematics 1, 2.
USERXTAL	User Crystal. Line from the target system plug that can be used to to connect the user's active components to the emulator processor on-chip clock generator circuit. Schematic 2.

* indicates signal source.

Table 8-3. Logic Symbols

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term.)

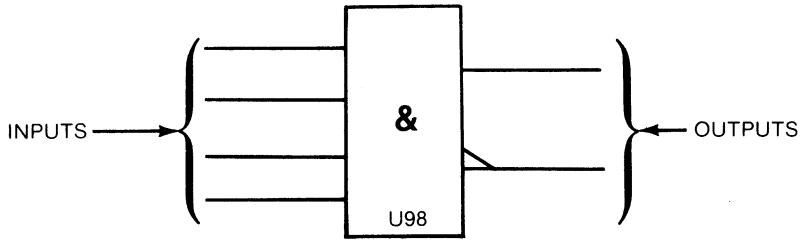
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

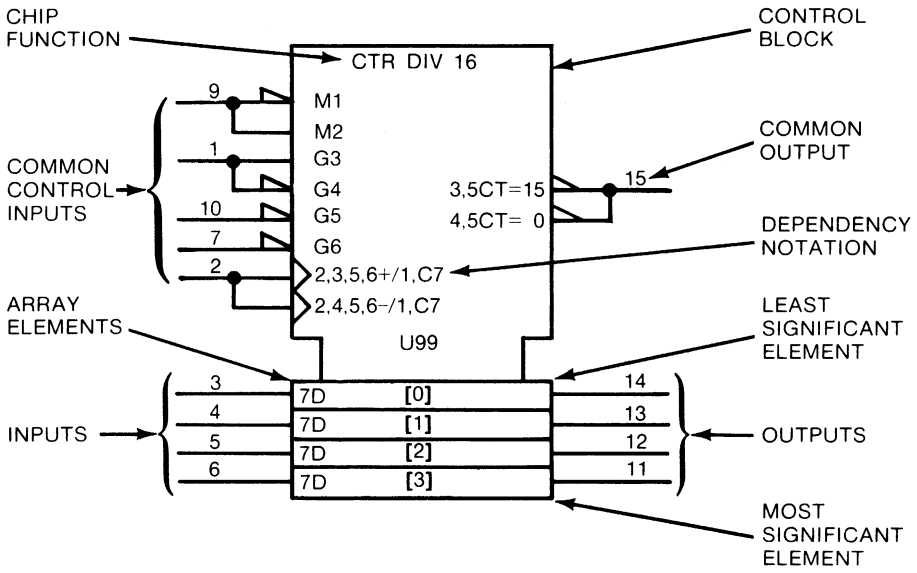
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. Unless indicated, the least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in **[ ]**).

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Table 8-3. Logic Symbols (Cont'd)

INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.

b. Interconnection (Z) indicates connections inside the symbol.

c. Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.

d. Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.

e. Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).

f. Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.

g. Address (A) identifies the address inputs.

h. Transmission (X) identifies bi-directional inputs and outputs that are connected together when the transmission input is true.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (compliments state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection
		X	Transmission

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Table 8-3. Logic Symbols (Cont'd)

OTHER SYMBOLS

Analog Signal	Inversion	→ Shift Right (or down)
& AND	O Negation	/ Solidus (allows an input or output to have more than one function)
Bit Grouping	Nonlogic Input/Output	▽ Tri-State
Buffer	Open Circuit (external resistor)	, Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.
! Compare	Open Circuit (external resistor)	
Dynamic	≥1 OR	( ) Used for factoring terms using algebraic techniques.
=1 Exclusive OR	Passive Pull Down (internal resistor)	[ ] Information not defined.
Hysteresis	Passive Pull Up (internal resistor)	Φ Logic symbol not defined due to complexity.
? Interrogation	Postponed	
— Internal Connection	← Shift Left (or up)	

LABELS

BG	Borrow Generate	CO	Carry Output	J	J Input
BI	Borrow Input	CP	Carry Propagate	K	K Input
BO	Borrow Output	CT	Content	P	Operand
BP	Borrow Propagate	D	Data Input	T	Transition
CG	Carry Generate	E	Extension (input or output)	+	Count Up
CI	Carry Input	F	Function	–	Count Down

MATH FUNCTIONS

Σ	Adder	>	Greater Than
ALU	Arithmetic Logic Unit	<	Less Than
COMP	Comparator	CPG	Look Ahead Carry Generator
DIV	Divide By	π	Multiplier
=	Equal To	P-Q	Subtractor

CHIP FUNCTIONS

BCD	Binary Coded Decimal	DIR	Directional	RAM	Random Access Memory
BIN	Binary	DMUX	Demultiplexer	RCVR	Line Receiver
BUF	Buffer	FF	Flip-Flop	ROM	Read Only Memory
CTR	Counter	MUX	Multiplexer	SEG	Segment
DEC	Decimal	OCT	Octal	SRG	Shift Register

DELAY and MULTIVIBRATORS

	Astable
100 ns	Delay
1	Nonretriggerable Monostable
NV	Nonvolatile
	Retriggerable Monostable

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Table 8-4. Schematic Diagram Notes

ETCHED CIRCUIT BOARD

FRONT PANEL MARKING

REAR-PANEL MARKING

MANUAL CONTROL

SCREWDRIVER ADJUSTMENT

TP1 ELECTRICAL TEST POINT TP (WITH NUMBER)

NUMBERED WAVEFORM NUMBER CORRESPONDS TO ELECTRICAL TEST POINT NO.

LETTERED TEST POINT NO MEASUREMENT AID PROVIDED

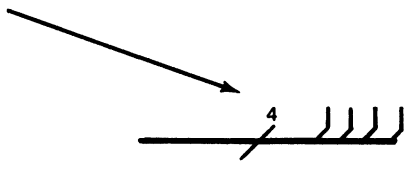
COMMON CONNECTIONS. ALL LIKE-DESIGNATED POINTS ARE CONNECTED.

1 3 NUMBER ON WHITE BACKGROUND = OFF-PAGE CONNECTION. LARGE NUMBER ADJACENT = SERVICE SHEET NUMBER FOR OFF-PAGE CONNECTION.

A CIRCLED LETTER = OFF-PAGE CONNECTION BETWEEN PAGES OF SAME SERVICE SHEET.

INDICATES SINGLE SIGNAL LINE

NUMBER OF LINES ON A BUS



(925) WIRE COLORS ARE GIVEN BY NUMBERS IN PARENTHESES USING THE RESISTOR COLOR CODE

[(925) IS WHT-RED-GRN]

0 - BLACK	5 - GREEN
1 - BROWN	6 - BLUE
2 - RED	7 - VIOLET
3 - ORANGE	8 - GRAY
4 - YELLOW	9 - WHITE

* OPTIMUM VALUE SELECTED AT FACTORY, TYPICAL VALUE SHOWN; PART MAY HAVE BEEN OMITTED.

UNLESS OTHERWISE INDICATED:
RESISTANCE IN OHMS
CAPACITANCE IN PICOFARADS
INDUCTANCE IN MICROHENRIES

μP	=	MICROPROCESSOR
P/O	=	PART OF
NC	=	NO CONNECTION
CW	=	CLOCKWISE END OF VARIABLE RESISTOR

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Table 8-5. IC to Schematics Cross-Reference.

Assembly A1 Lower Board.

IC	Schematic
A1 U1A	4
A1 U1B	4
A1 U1C	3
A1 U1E	4
A1 U1F	3
A1 U1G	3
A1 U1H	3
A1 U2A	3, 4
A1 U2B	3
A1 U2C	3, 4
A1 U2D	3, 4
A1 U2E	4
A1 U2F	4
A1 U2G	3
A1 U2H	3
A1 U3A	4
A1 U3B	4
A1 U3C	4
A1 U3D	4
A1 U3E	4
A1 U3F	3
A1 U3G	3
A1 U3H	3

Assembly A2 Upper Board.

IC	Schematic
A2 U1A	2
A2 U1B	2
A2 U1C	2
A2 U1D	2
A2 U2A	2
A2 U2B	2
A2 U2C	2
A2 U2D	2
A2 U2E	1
A2 U2F	1
A2 U2G	1
A2 U2H	1

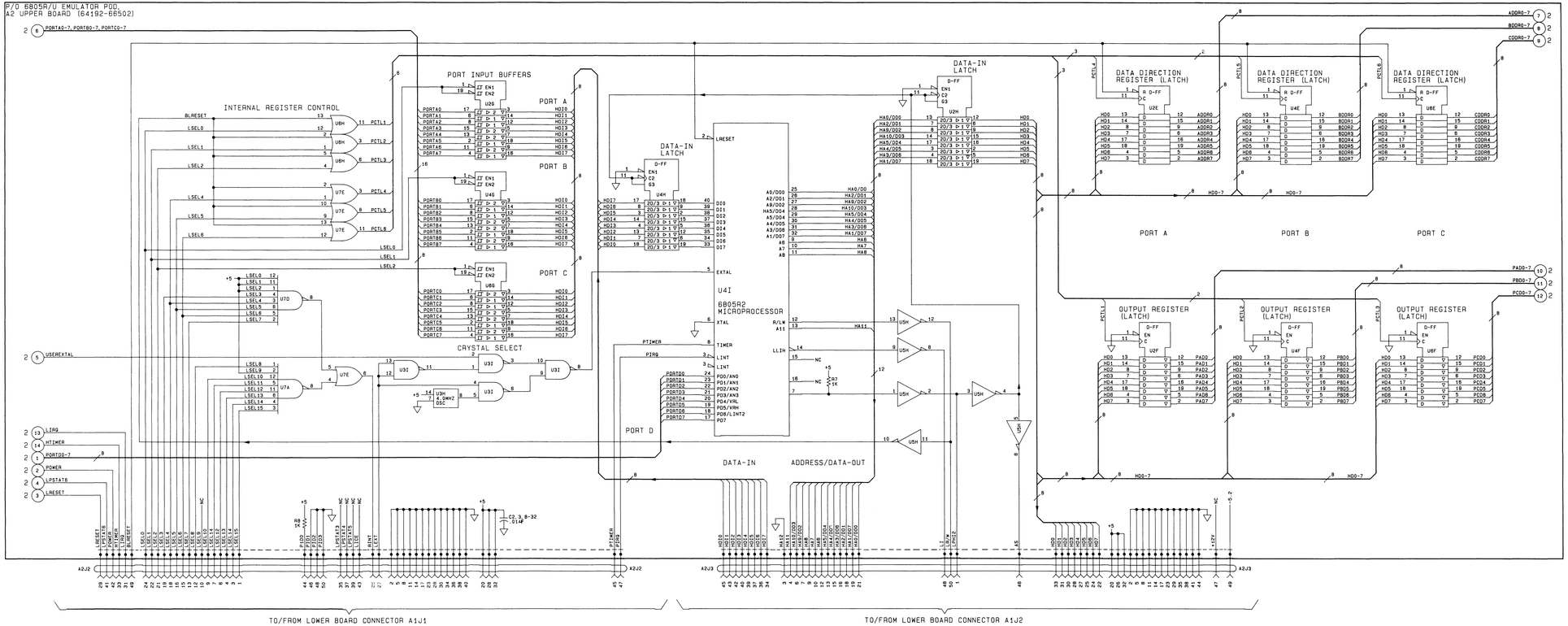
Assembly A2 Continued

IC	Schematic
A2 U3A	2
A2 U3B	2
A2 U3C	2
A2 U3D	2
A2 U3H	1
A2 U3I	1
A2 U4A	2
A2 U4B	2
A2 U4C	2
A2 U4D	2
A2 U4E	1
A2 U4F	1
A2 U4G	1
A2 U4H	1
A2 U4I	1
A2 U5A	2
A2 U5B	2
A2 U5C	2
A2 U5D	2
A2 U5H	1
A2 U6B	2
A2 U6C	2
A2 U6D	2
A2 U6E	1
A2 U6F	1
A2 U6G	1
A2 U6H	1
A2 U7A	1
A2 U7D	1
A2 U7E	1

Assembly A3 Probe

A3 U1	in plug


TO TARGET SYSTEM
J1
U1A
U1B
U1C
U1D
U2A
U2B
U2C
U2D
U2E
U2F
U2G
U2H
U3A
U3B
U3C
U3D
U3H
U3I
U4A
U4B
U4C
U4D
U4E
U4F
U4G
U4H
U4I
U5A
U5B
U5C
U5D
U5H
U6B
U6C
U6D
U6E
U6F
U6G
U6H
U7A
U7D
U7E
J2
J3
C0002
1 of 2
MP1
MP2
MP3
MP4
U1E
U1F
U1G
U1H
RP1
RP2
YELLOW DOT
RED DOT
MP5
MP6
MP7
MP8
J4
(TO CONTROL BOARD IN MAINFRAME) POD BUS
C0002
2 of 2



1

ICs On This Schematic

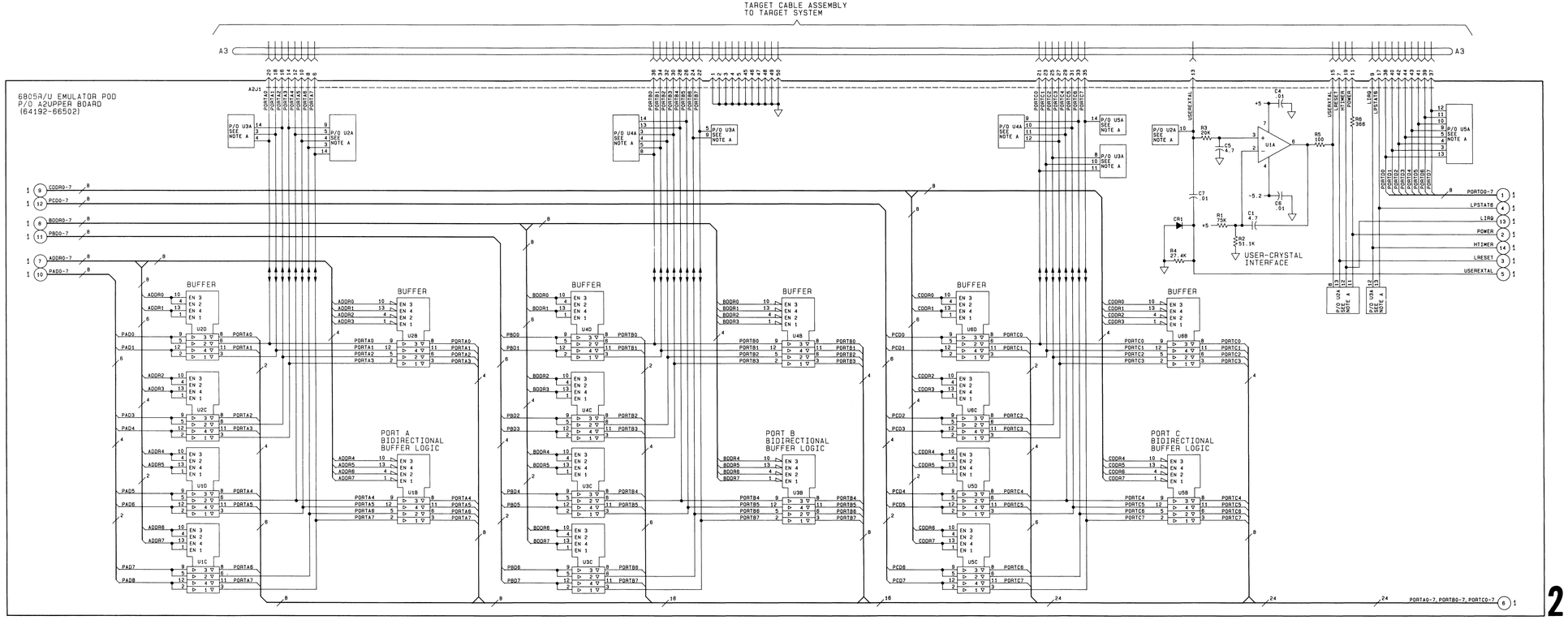
REF DES	HP PART NUMBER	MFG. PART NUMBER	+5V PIN	GND PIN
A2 U2E	1820-1730	SN74LS273N	20	10
A2 U2F	1820-1997	SN74LS374N	20	10
A2 U2G	1820-2024	SN74LS244N	20	10
A2 U2H	1820-2102	SN74LS373N	20	10
A2 U3H	1813-0174	1813-0174	14	7
A2 U3I	1820-1197	SN74LS00N	14	7
A2 U4E	1820-1730	SN74LS273N	20	10
A2 U4F	1820-1997	SN74LS374N	20	10
A2 U4G	1820-2024	SN74LS244N	20	10
A2 U4H	1820-2102	SN74LS373N	20	10
A2 U4I	1820-2930	1820-2930	4	1
A2 U5H	1820-1199	SN74LS04N	14	7
A2 U6E	1820-1730	SN74LS273N	20	10
A2 U6F	1820-1997	SN74LS374N	20	10
A2 U6G	1820-2024	SN74LS244N	20	10
A2 U6H	1820-2108	SN74LS32N	14	7
A2 U7A	1820-1207	SN74LS30N	14	7
A2 U7D	1820-1207	SN74LS30N	14	7
A2 U7E	1820-1208	SN74LS32N	14	7

Parts On This Schematic

A2 C2,3,8-32.	R8,7.

Figure 8-6. Schematic 1
Upper Board Assembly A2

Component Locator
Upper Board, Assembly A2



ICs On This Schematic

REF DES	HP PART NUMBER	MFG PART NUMBER	+5V PIN	GND PIN
A2 U1A	1820-0217	1820-0217	7	na
A2 U1B	1820-1568	SN74LS125AN	14	7
A2 U1C	1820-1645	SN74LS126AN	14	7
A2 U1D	1820-1645	SN74LS126AN	14	7
A2 U2A	1906-0202	TID130	2,6	1,7
A2 U2B	1820-1568	SN74LS125AN	14	7
A2 U2C	1820-1645	SN74LS126AN	14	7
A2 U2D	1820-1645	SN74LS126AN	14	7
A2 U3A	1906-0202	TID130	2,6	1,7
A2 U3B	1820-1568	SN74LS125AN	14	7
A2 U3C	1820-1645	SN74LS126AN	14	7
A2 U3D	1820-1645	SN74LS126AN	14	7
A2 U4A	1906-0202	TID130	2,6	1,7
A2 U4B	1820-1568	SN74LS125AN	14	7
A2 U4C	1820-1645	SN74LS126AN	14	7
A2 U4D	1820-1645	SN74LS126AN	14	7
A2 U5A	1906-0202	TID130	2,6	1,7
A2 U5B	1820-1568	SN74LS125AN	14	7
A2 U5C	1820-1645	SN74LS126AN	14	7
A2 U5D	1820-1645	SN74LS126AN	14	7
A2 U6B	1820-1568	SN74LS125AN	14	7
A2 U6C	1820-1645	SN74LS126AN	14	7
A2 U6D	1820-1645	SN74LS126AN	14	7

Parts On This Schematic

A2 C1,4,5,6,7.	A2 CR1.
A2 R1,2,3,4,5,6.	

NOTE A

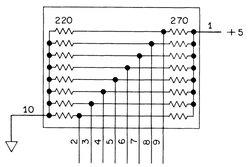
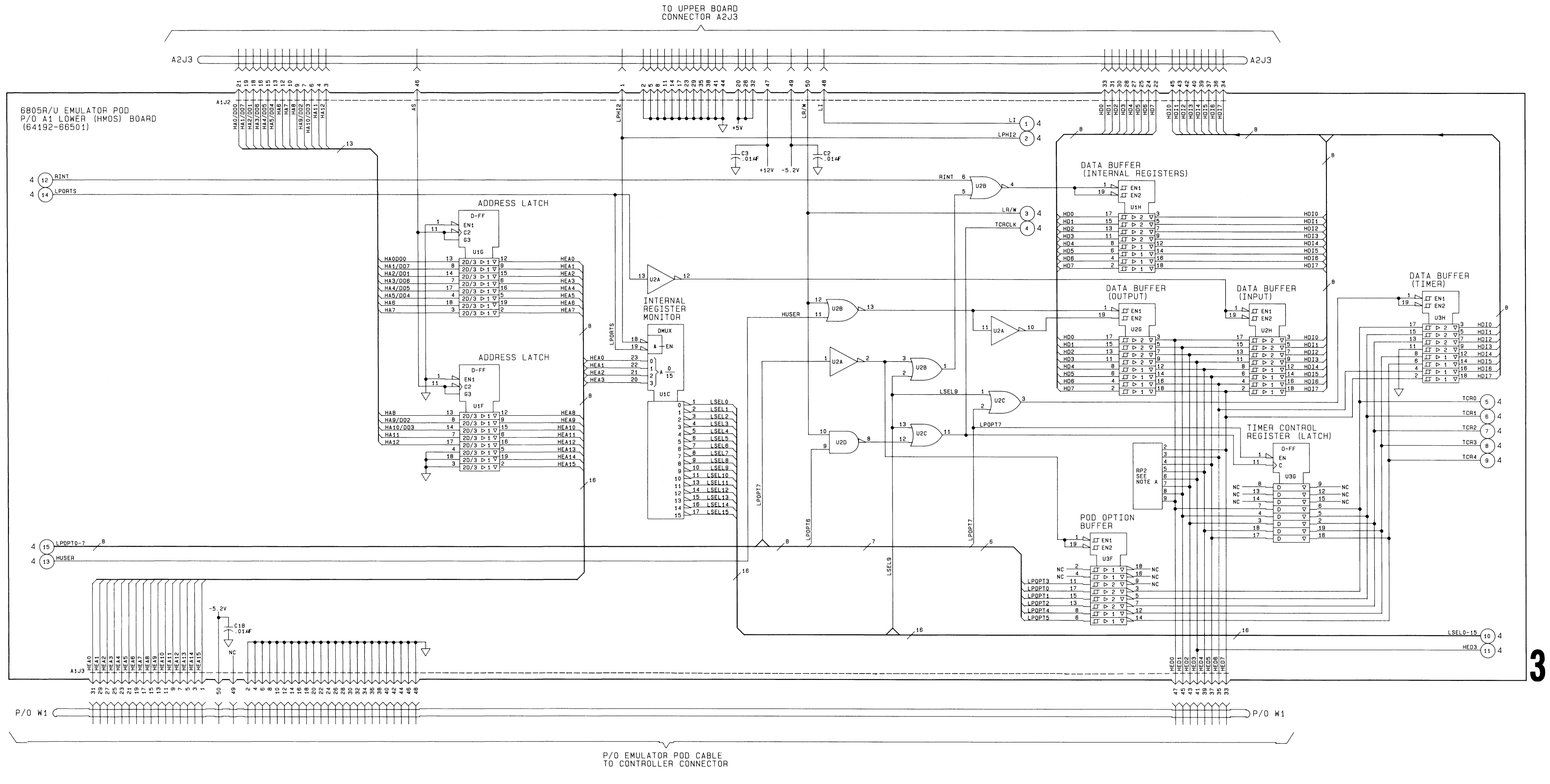


Figure 8-7. Schematic 2
Upper Board Assembly A2

Component Locator
Lower Board, Assembly A1



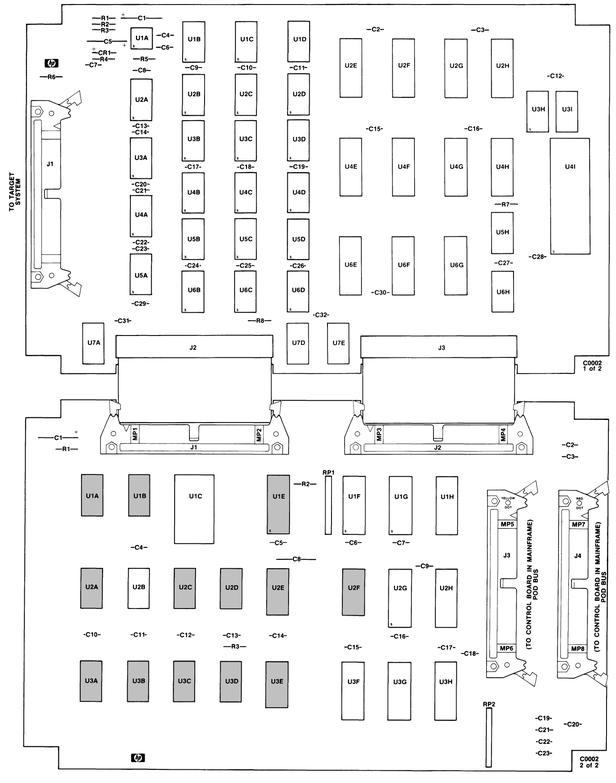
ICs On This Schematic

REF DES	HP PART NUMBER	MFG PART NUMBER	+5V PIN	GND PIN
A1 U1C	1820-0495	SN74154N	24	12
A1 U1F	1820-1676	SN74S373N	20	10
A1 U1G	1820-1676	SN74S373N	20	10
A1 U1H	1820-2024	SN74LS244N	20	10
A1 U2A	1820-1199	SN74LS04N	14	7
A1 U2B	1820-1144	SN74LS02N	14	7
A1 U2C	1820-1208	SN74LS32N	14	7
A1 U2D	1820-1197	SN74LS00N	14	7
A1 U2G	1820-1624	SN74S241N	20	10
A1 U2H	1820-2024	SN74LS244N	20	10
A1 U3F	1820-1917	SN74LS240N	20	10
A1 U3G	1820-1997	SN74LS374N	20	10
A1 U3H	1820-2024	SN74LS244N	20	10

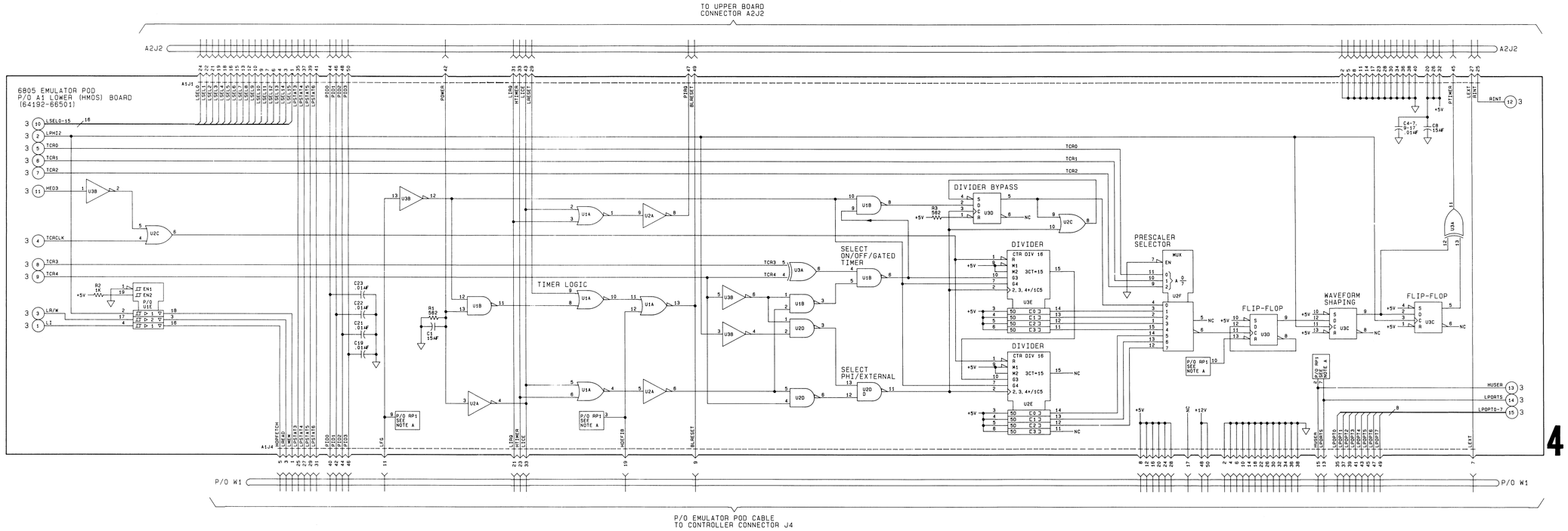
Parts On This Schematic

A1 C2,3,18.	RP2.

Figure 8-8. Schematic 3
Lower Board, Assembly A1



Component Locator
Lower Board, Assembly A1



4

ICs On This Schematic

REF DES	HP PART NUMBER	MFG PART NUMBER	+5V PIN	GND PIN
A1 U1A	1820-1144	SN74LS02N	14	7
A1 U1B	1820-1197	SN74LS00N	14	7
A1 U1E	1820-1624	SN74S241N	20	10
A1 U2A	1820-1199	SN74LS04N	14	7
A1 U2C	1820-1208	SN74LS32N	14	7
A1 U2D	1820-1197	SN74LS00N	14	7
A1 U2E	1820-1430	SN74LS161AN	16	8
A1 U2F	1820-1217	SN74LS151N	16	8
A1 U3A	1820-1211	SN74LS86N	14	7
A1 U3B	1820-1199	SN74LS04N	14	7
A1 U3C	1820-1112	SN74LS74AN	14	7
A1 U3D	1820-1112	SN74LS74AN	14	7
A1 U3E	1820-1430	SN74LS161AN	16	8

Parts On This Schematic

A1 C1,4-17,19-23. A1 R2,3. A1 RP1.

NOTE A

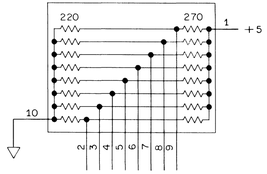


Figure 8-9. Service Sheet 4
Lower Board Assembly A1
8-31

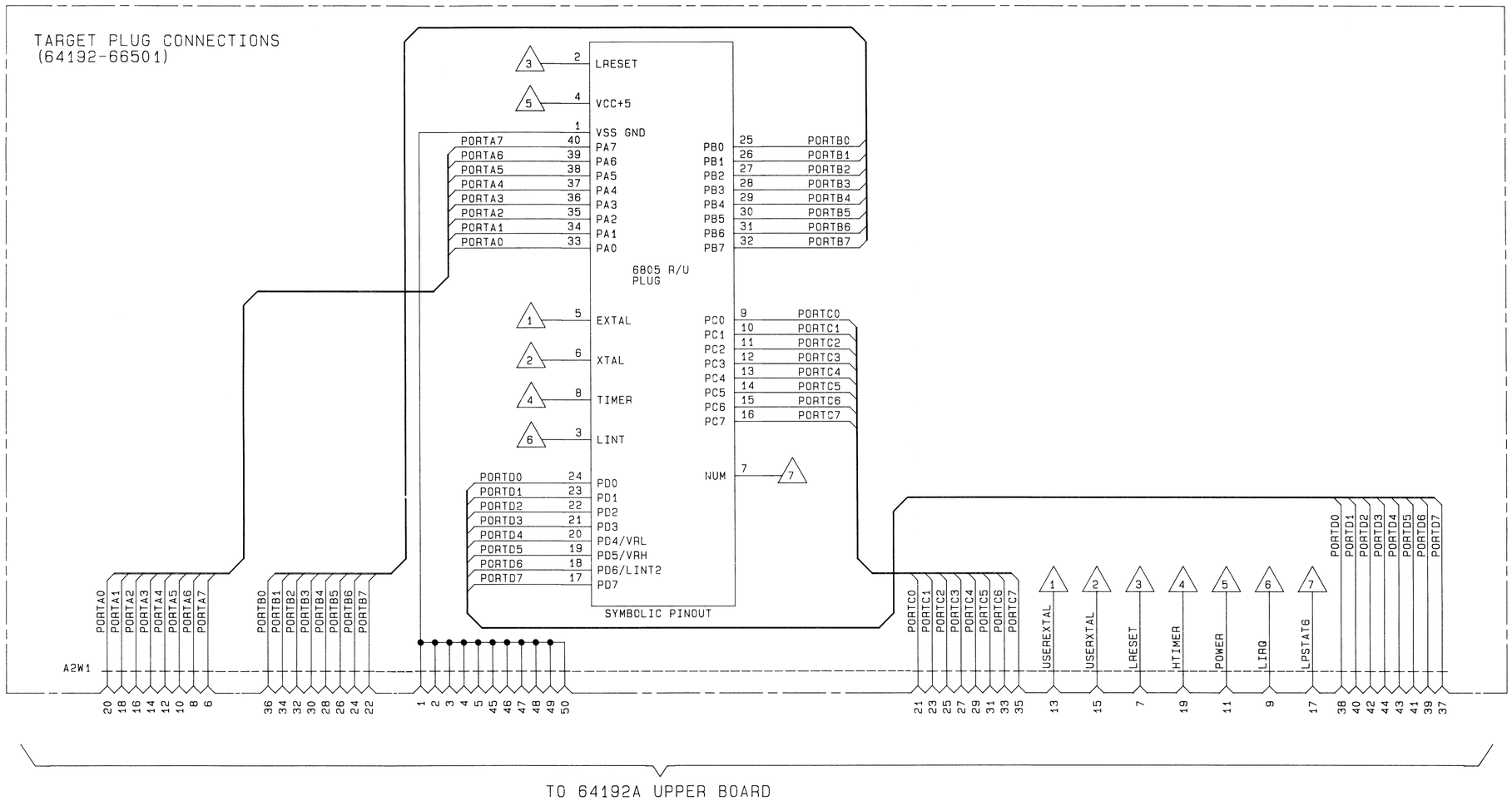


Figure 8-10. Schematic 5
Target Plug Connections

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Key	Product Line
A	Analytical
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MP	Medical Products Primary SRO
MS	Medical Products Secondary SRO
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**	Support only for specific product line

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Telex: 215238
E,C

Hewlett-Packard Italiana S.p.A.
Via Turazza 14
I-35100 **PADOVA**
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A,CH,E,MS

Hewlett-Packard Italiana S.p.A.
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Telex: 610514
A,CH,CM,CS,E,MS,P*

Hewlett-Packard Italiana S.p.A.
Corso Svizzera, 184
I-10149 **TORINO**
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Telex: 221079
CH,E

JAPAN

Yokogawa-Hewlett-Packard Ltd.
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000 **ATSUGI**, Kanagawa, 243
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CM,C*,E

Yokogawa-Hewlett-Packard Ltd.
Towa Building
2-3, Kaigan-dori, 2 Chome Chuo-ku
KOBE, 650
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C,E

Yokogawa-Hewlett-Packard Ltd.
Kumagaya Asahi 82 Bldg
3-4 Tsukuba
KUMAGAYA, Saitama 360
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CH,CM,E

Yokogawa-Hewlett-Packard Ltd.
Asahi Shinbun Daiichi Seimei Bldg.
4-7, Hanabata-cho
KUMAMOTO,860
Tel: (0963) 54-7311
CH,E

Yokogawa-Hewlett-Packard Ltd.
Shin-Kyoto Center Bldg.
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Karasuma-Nishiiru
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KYOTO, 600
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Yokogawa-Hewlett-Packard Ltd.
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NAGOYA, 450
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Yokogawa-Hewlett-Packard Ltd.
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7-1, Nishi Shinjuku, 2 Chome
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CH,E,M,P

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KOREA

Samsung Electronics Computer Division
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Telex: 22481 Areeg kt
CH,E,M

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P

LEBANON

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Woluwedal
B-1200 **BRUSSELS**
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Tel: 36299
Telex: MA 70904 PROTEL
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P

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E

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P

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OMAN

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P

Suhail & Saud Bahwan
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Telex: 2894 MUSKO PK
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Calle Samuel Lewis, Ed. Alfa
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Telex: 3483 ELECTRON PG
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CM,E,M,P

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Tel: 85-35-81, 85-34-91, 85-32-21
Telex: 3274 ONLINE
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Telex: 40018, 42000 ITT GLOBE MACKAY BOOTH
P

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Mundinter
Intercambio Mundial de Comércio S.A.R.L.
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M

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Telex: 13316 SABASA
P

Telectra-Empresa Técnica de Equipmentos Eléctricos S.A.R.L.
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P

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Nasser Trading & Contracting
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DOHA
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Telex: 4439 NASSER DH
M

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CH,CS,E,M,P

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CM

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Crta. de la Coruña, Km. 16, 400
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Hewlett-Packard Sverige AB
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CH-8967 **WIDEN**
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E

Middle East Electronics
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M,P

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A

THAILAND

Unimesa
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Telex: 84439 Simonco TH
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Bangkok Business Equipment Ltd.
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P

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M

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*Kavaklidere, **ANKARA***
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E

E.M.A.
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92123
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